

Compal Confidential

Model Name : Charmander_UMA
Compal Project Name : C5V01 / D7W01
File Name : LA-E891P

Compal Confidential
C5V01 MB Schematic Document
LA-E891P

Rev: 1A
2017.06.12

Security Classification		Compal Secret Data		Compal Electronics, Inc.	
Issued Date	2016/11/04	Deciphered Date	2018/11/04	Title Cover Sheet	
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HDMI Conn.



page 22

DDI1
HDMI x 4 lanes

eDP



page 21

eDP

DDI

eMMC

eMMC

page 27



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PCIe 3.0 x4
8GT/s
Port 9-12Flexible IO
Base-U PCIe2.0
Premium-U PCIe3.0

Intel Kabylake U

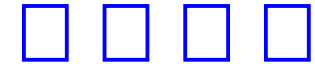
Kabylake U
Kabylake PCH-LP(MCP)
(KBL-U_2+2)
(KBL-RU_4+2)

Processor

Dual Core + GT2
Quad Core + GT2

Interleaved Memory

DDR4-ON BOARD 4G 8Gb x16



page 19

260pin DDR4-SO-DIMM X1



page 20

Memory BUS
Dual Channel

1.2V DDR4 1866/2133

USB 3.0
conn x1
USB port 1

page 29

USB 2.0
conn x2
USB port3,4
on Sub/B

page 29

CMOS
Camera
USB port 7

page 21

USB TypeC
conn x1
USB (port 2,3)

page 28

Fingerprint

USB port8
page 31USBx8
48MHz

HD Audio

3.3V 24MHz

HDA Codec
ALC255
page 25Touch
ScreenUSB port 6
page 21

SPI

SPI ROM
64Mb
page 9

SMBUS

Sensor
page 26

LPC/eSPI BUS

CLK=24MHz

ENE
KB9022
page 30TPM
page 31

Int.KBD



page 31

Touch Pad
PS2 (from EC) / I2C (from SOC)

page 31

Int. Speaker
page 25Int. DMIC
on Camera
page 21UAI
on Sub/B
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vinafix

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2016/11/04		2018/11/04		Title	
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				C5V01 M/B LA-E891P	
Date: Monday, June 12, 2017		Sheet 2 of 46			

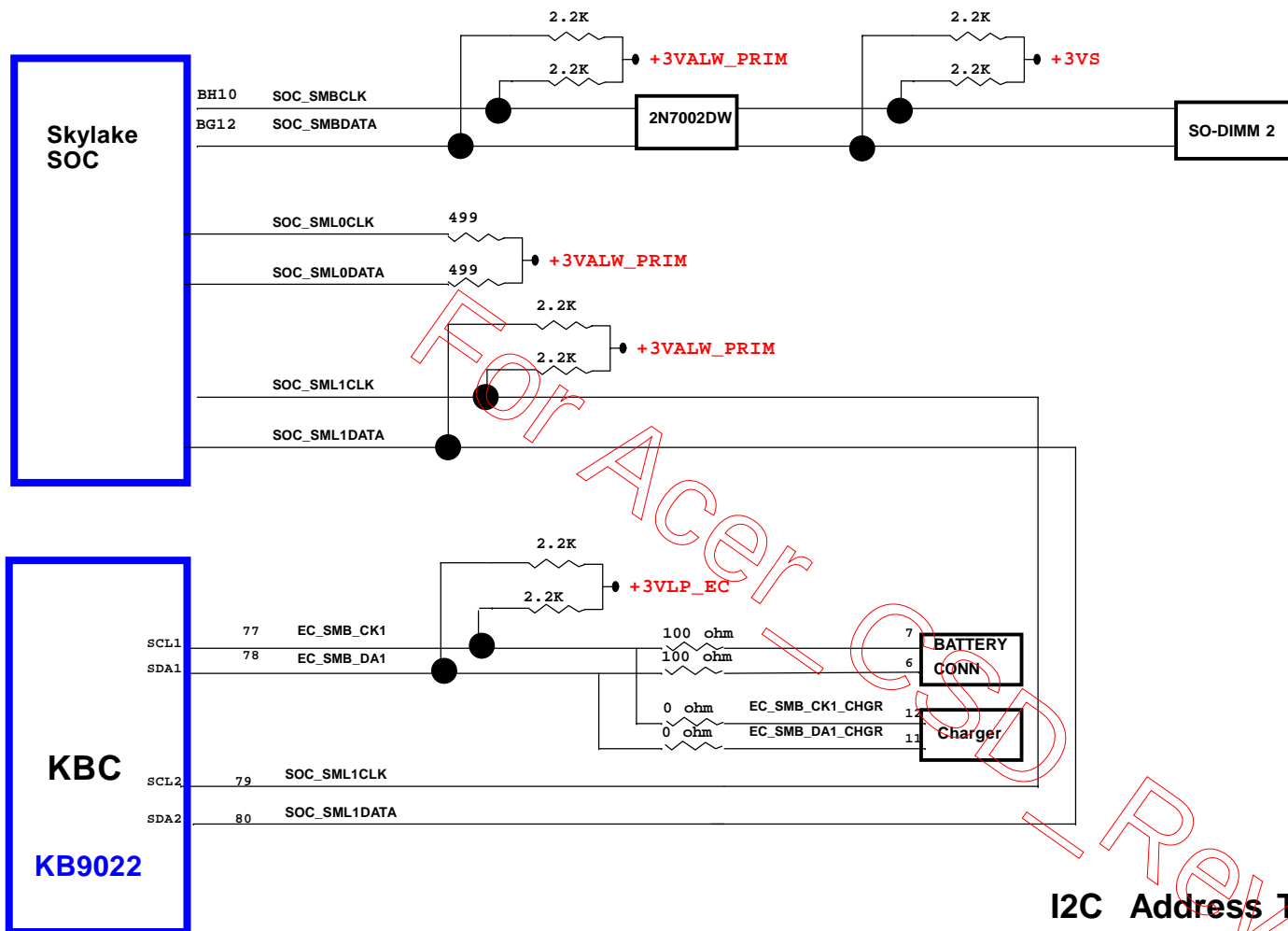
Vcc	3.3V +/- 5%					
Ra	100K +/- 1%					
Board ID	Rb	V _{SD} min	V _{SD} typ	V _{SD} max	EC AD3	PCB Revision
0	0	0 V	0 V	0.300 V	0x00 - 0x13	0.1 (EVT)
1	12K +/- 1%	0.347 V	0.345 V	0.360 V	0x14 - 0x1E	1.0 (DVT)
2	15K +/- 1%	0.423 V	0.430 V	0.438 V	0x1F - 0x25	1A (PVT)
3	20K +/- 1%	0.541 V	0.550 V	0.559 V	0x26 - 0x30	1A (MP)
4	27K +/- 1%	0.691 V	0.702 V	0.713 V	0x31 - 0x3A	D7W01 (PVT)
5	33K +/- 1%	0.807 V	0.819 V	0.831 V	0x3B - 0x45	D7W01 (MP)
6	43K +/- 1%	0.978 V	0.992 V	1.006 V	0x46 - 0x54	
7	56K +/- 1%	1.169 V	1.185 V	1.200 V	0x55 - 0x64	

BOM Option Table		BOM Option Table	
Item	BOM Structure	Item	BOM Structure
Unpop	@	MB Stage	EVT@/DVT@/PVT@/MP@
Connector	CONN@	BOM Select	X76@
Acer BYOC	BYOC@ / NBYOC@	Memory Select	X76M01@~ X76M03@
CODEC(ALC255)	255@	Memory Mode	SDR@ / DDR@
EC Mode Select	LPC@ / ESPI@	SATA Redriver Select	X76TH@ / X76PAR@
For Intel CMC	CMC@	DAZ PN	DAZ@
LAN Mode Select	SWR@ / LDO@	PCB PN	PCB@
EMI requirement	EMI@ / @EMI@	HDMI LOGO	45@
ESD requirement	ESD@ / @ESD@		
RF requirement	@RF@		
CPU Selection	U42@/U22@		
TPM	TPM@		
Finger Print	FP@		
UMA or DGPU	UMA@/VGA@		
ODD Support	ODD@		
G Sensor	BA@		
For over 3 cell battery	3S@	CPU Code	QKIW@

43	Level	Description	BOM Structure
431A72B0L01	SMT MB AE891 C5V01 UMA I36006U HDMI	SR2UW@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L02	SMT MB AE891 C5V01 UMA I3 QLPD1.4 HDMI	QLDP@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L03	SMT MB AE891 C5V01 UMA I5 QLD1.4 HDMI	QLDM@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L04	SMT MB AE891 C5V01 UMA I7 QLDN1.4 HDMI	QLDN@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L05	SMT MB AE891 C5V01 UMA I3 QLYK2.2 HDMI	QLYK@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L06	SMT MB AE891 C5V01 UMA I3-7100 1.4 HDMI	Q37100@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L07	SMT MB AE891 C5V01 UMA I5 QLYJ2.2 HDMI	QLYJ@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L08	SMT MB AE891 C5V01 UMA I5-7200 1.4 HDMI	I57200@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L09	SMT MB AE891 C5V01 UMA I7 QLYH2.2 HDMI	QLYH@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L10	SMT MB AE891 C5V01 UMA I7 QLYH2.2 HDMI	I77500@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L11	SMT MB AE891 C5V01 UMA I3-7100 2.2 HDMI	I3710022@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
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431A72B0L14	SMT MB AE891 C5V01 UMA I3-7100 U42 HDMI	I3710022@/CMC@/LPC@/UMA@/U42@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L15	SMT MB AE891 C5V01 UMA I5 QN5D U42 HDMI	QN5D@/CMC@/LPC@/UMA@/U42@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L16	SMT MB AE891 C5V01 UMA I7 QN5C U42 HDMI	QN5C@/CMC@/LPC@/UMA@/U42@/3S@/LDO@/NBYOC@/255@/CHG@/MP@/X4E@/X76M@/DAZE@/X76PAR@/C5V01@	
431A72B0L51	SMT MB AE891 C5V01 UMA I7 QN5C U42 HDMI	SR2UW@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/EAL7PVT@/X4E@/X76M@/EAL7DAZE@/X76PAR@/D7W01@/O	
431A72B0L52	SMT MB AE891 D7W01 UMA I3-6006 HDMI	I3710022@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/EAL7PVT@/X4E@/X76M@/EAL7DAZE@/X76PAR@/D7W01@	
431A72B0L53	SMT MB AE891 D7W01 UMA I5-7200 HDMI	I5720022@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/EAL7PVT@/X4E@/X76M@/EAL7DAZE@/X76PAR@/D7W01@	
431A72B0L54	SMT MB AE891 D7W01 UMA I7-7500 HDMI	I7750022@/CMC@/LPC@/UMA@/U22@/3S@/LDO@/NBYOC@/255@/CHG@/EAL7PVT@/X4E@/X76M@/EAL7DAZE@/X76PAR@/D7W01@	
431A72B0L55	SMT MB AE891 D7W01 UMA QNEF HDMI	U4215@/CMC@/LPC@/UMA@/U42@/3S@/LDO@/NBYOC@/255@/CHG@/EAL7PVT@/X4E@/X76M@/EAL7DAZE@/X76PAR@/D7W01@/O	
431A72B0L56	SMT MB AE891 D7W01 UMA QNBF HDMI	U4215@/CMC@/LPC@/UMA@/U42@/3S@/LDO@/NBYOC@/255@/CHG@/EAL7PVT@/X4E@/X76M@/EAL7DAZE@/X76PAR@/D7W01@/O	

<i>STATE</i> \ <i>SIGNAL</i>	<i>SLP_S3#</i>	<i>SLP_S4#</i>	<i>SLP_S5#</i>	<i>+VALW</i>	<i>+V</i>	<i>+VS</i>	<i>Clock</i>
<i>S0 (Full ON)</i>	<i>HIGH</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>	<i>ON</i>
<i>S3 (Suspend to RAM)</i>	<i>LOW</i>	<i>HIGH</i>	<i>HIGH</i>	<i>ON</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>
<i>S4 (Suspend to Disk)</i>	<i>LOW</i>	<i>LOW</i>	<i>HIGH</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>
<i>S5 (Soft OFF)</i>	<i>LOW</i>	<i>LOW</i>	<i>LOW</i>	<i>ON</i>	<i>OFF</i>	<i>OFF</i>	<i>OFF</i>

Power Plane	Description	S0	S3	S4/S5
+19V_VIN	Adapter power supply	N/A	N/A	N/A
+17.4V_BATT	Battery power supply	N/A	N/A	N/A
+19VB	AC or battery power rail for power circuit.	N/A	N/A	N/A
+VCC_CORE	Processor IA Cores Power Rail	ON	OFF	OFF
+VCC_GT	Processor Graphics Power Rails	ON	OFF	OFF
+VCC_SA	System Agent power rail	ON	OFF	OFF
+0.6VS_VTT	DDR +0.6VS power rail for DDR terminator .	ON	OFF	OFF
+1.0VALW_PRIM	+1.0V Always power rail	ON	ON	ON*1
+1.0V_VCCSTU	Sustain voltage for processor in Standby modes	ON	ON	OFF
+VCCIO	CPU IO power rail	ON	OFF	OFF
+1.0VS_VCCSTG	+1.0VALW_PRIM Gated version of VCCST	ON	OFF	OFF
+1.2V_VDDQ	DDR4 +1.2V Power Rail	ON	ON	OFF
+1.8VALW_PRIM	+1.8V Always power rail	ON	ON	ON*1
+1.8VS	System +1.8V power rail	ON	OFF	OFF
+3VLP	+19VB to +3VLP power rail for suspend power	ON	ON	ON
+3VALW	System +3VALW always on power rail	ON	ON	ON*1
+3VS	System +3V power rail	ON	OFF	OFF
+5VALW	+5V Always power rail	ON	ON	ON
+5VS	System +5V power rail	ON	OFF	OFF
+RTCVCC	RTC Battery Power	ON	ON	ON

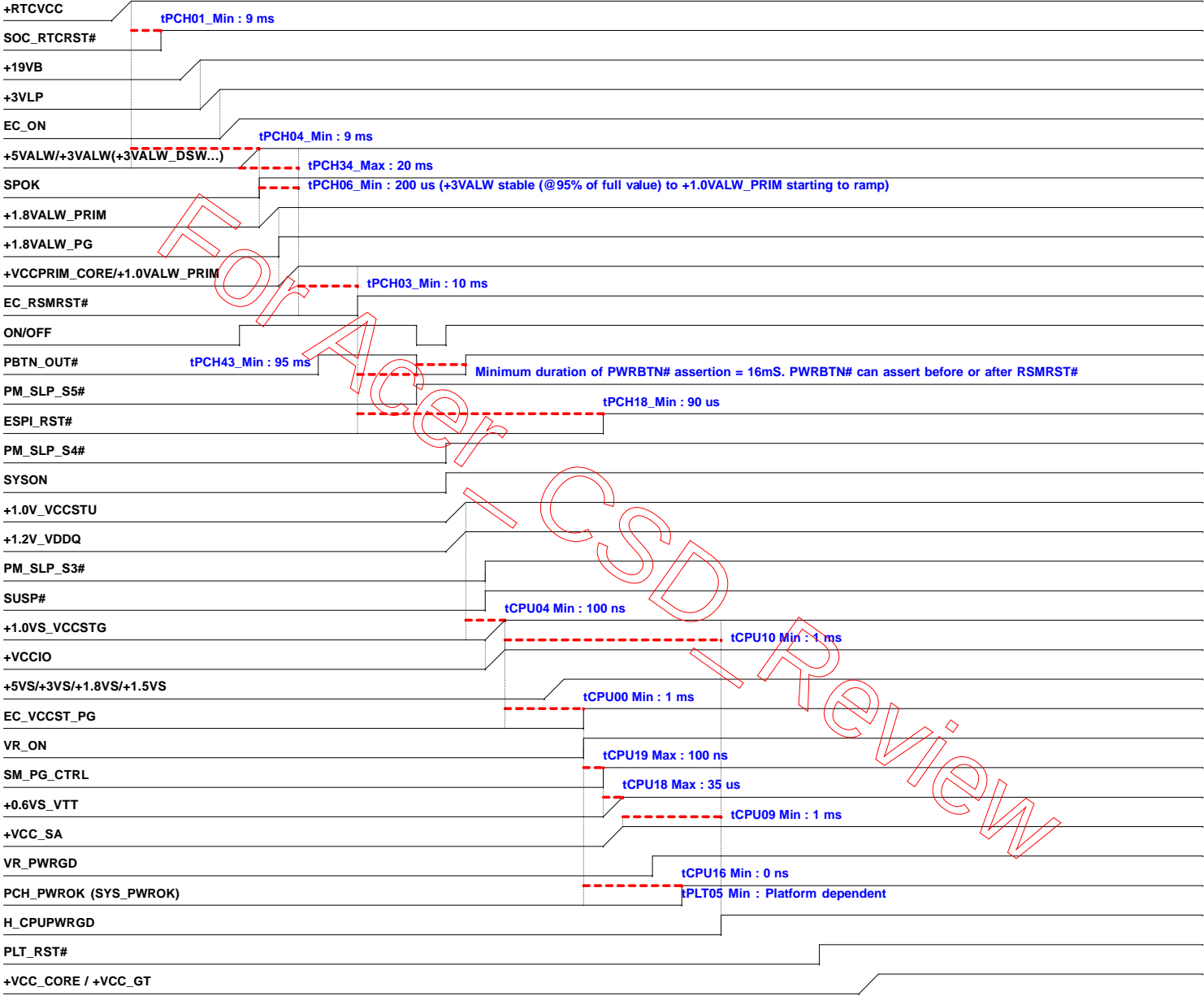


I2C Address Table

Need check

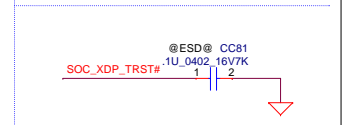
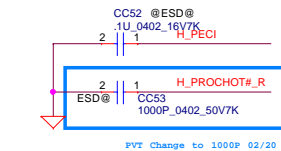
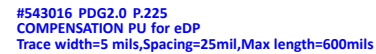
BUS	Device	Address(7 bit)	Address(8bit)	
			Write	Read
I2C_0 (+3VS)	Reserved (Touch Panel)			
I2C_1 (+3VS)	TM-P2969-001 (TP)	0x2C		
	SB8787-1200 (TP-ELAN)	0x15		
SOC_SMBCLK +3VS	DIMM2	0xA4		
SOC_SML1CLK +3VALW_PRIM	PCH-LP (SOC)	0x90		
EC_SMB_CK1 +3VLP	BQ24780 (Charger IC)	0x12		
	BATTERY PACK	0x16		

PWR Sequence_SKL-U2+2_DDR3L_Value_NON CS



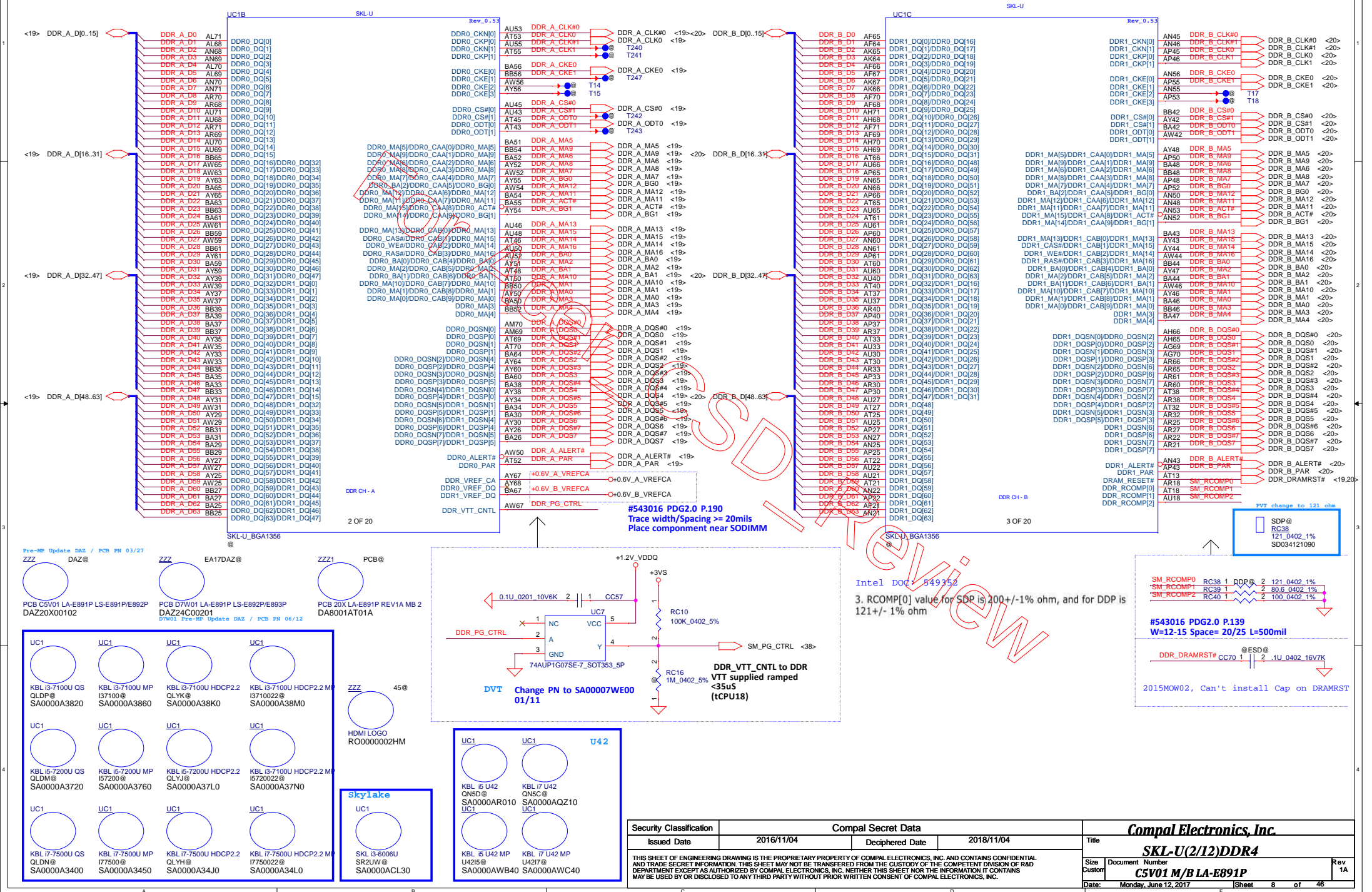
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Issued Date	2016/11/04	Deciphered Date	2018/11/04	Title		
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				Size	Document Number	Rev
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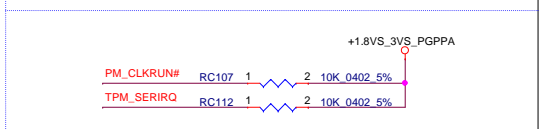
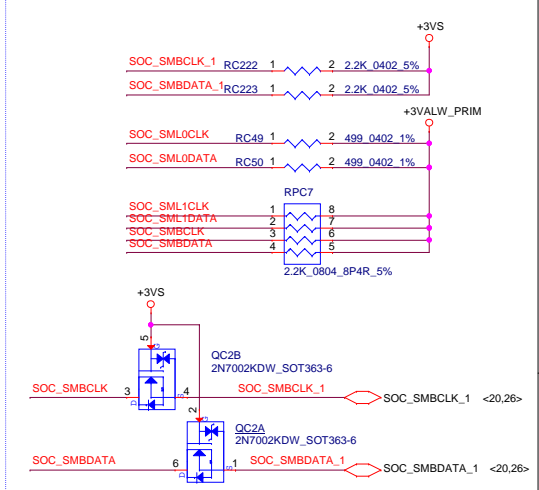
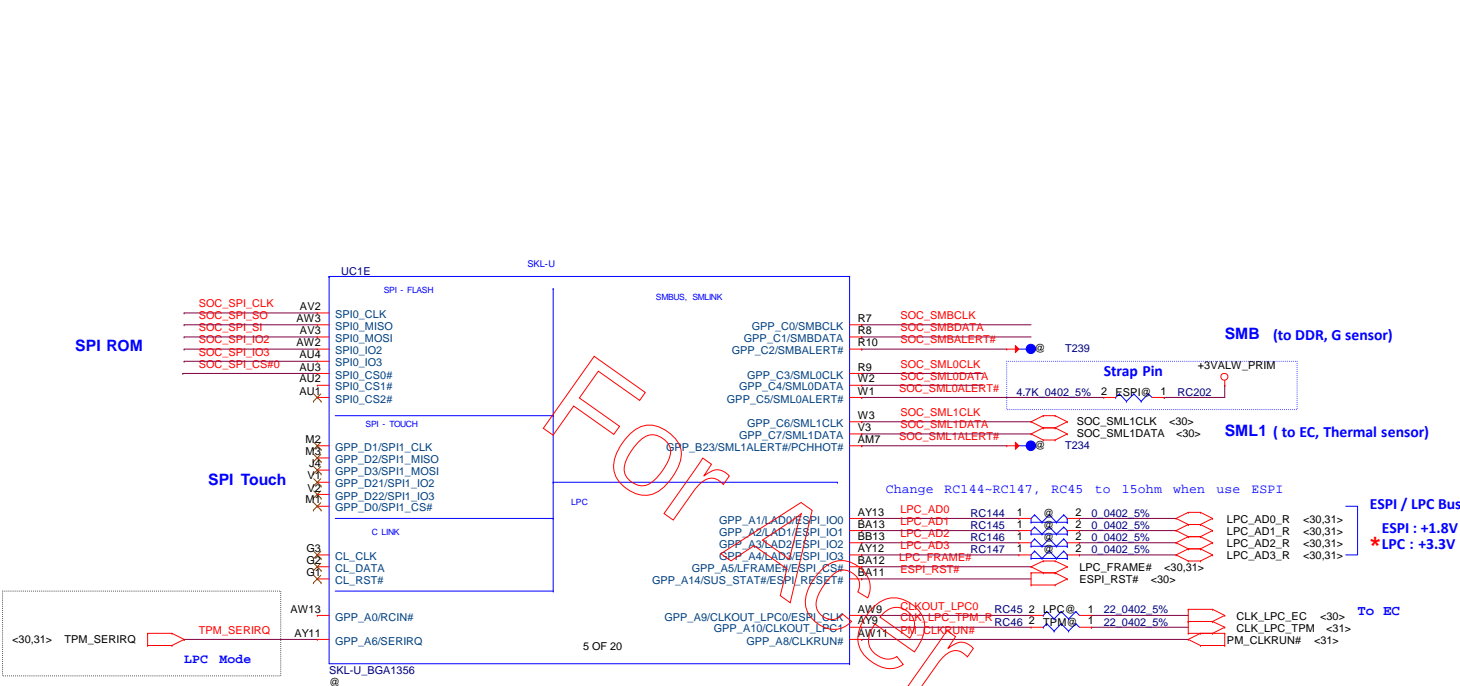
DDPB_CTRLDATA
DDPC_CTRLDATA
Display Port B/C Detected
NC =Port is not detected.
PU =Port is detected.



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				C5V01 M/B LA-E891P Date: Monday, June 12, 2017	Sheet 7 of 46

Interleaved Memory



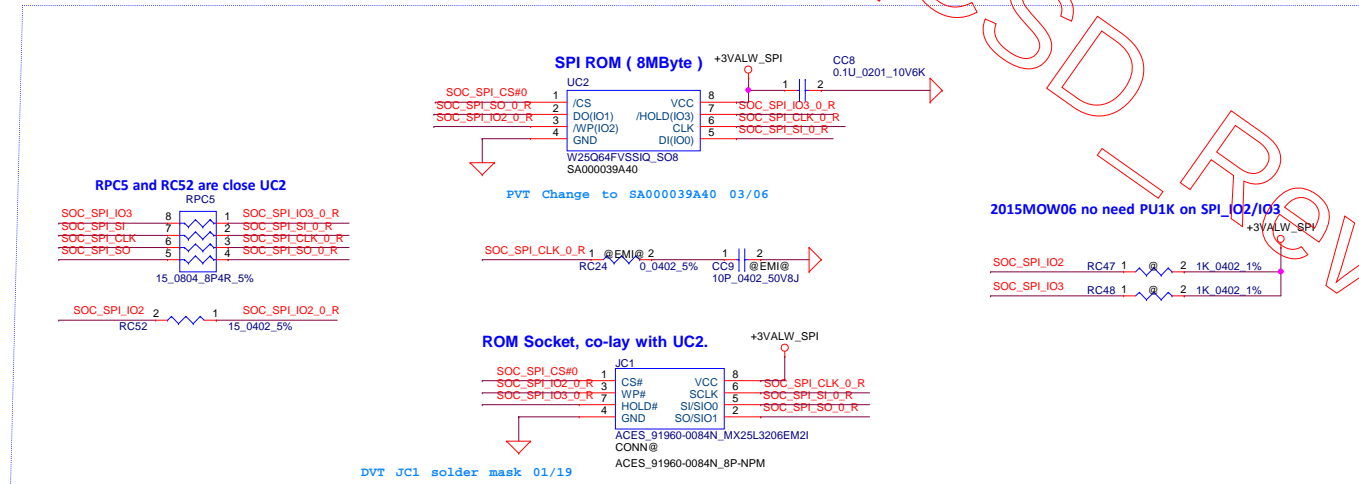


SML0ALERT# / GPP_C5 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

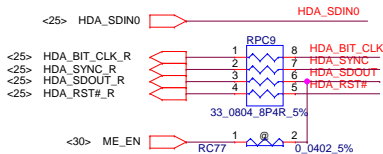
eSPI or LPC
* 0 = LPC is selected for EC --> For KB9022/9032 Use
1 = eSPI is selected for EC --> For KB9032 Only.

SMBALERT# / GPP_C2 (Internal Pull Down):
(Sampled: Rising edge of RSMRST#)

TLS Confidentiality
* 0 = Disable Intel ME Crypto Transport Layer Security (TLS) cipher suite (no confidentiality)
1 = Enable Intel ME Crypto (TLS) (with confidentiality). Must be pulled up to support Intel AMT with TLS and Intel SBA (Small Business Advantage) with TLS.



HDA for AUDIO

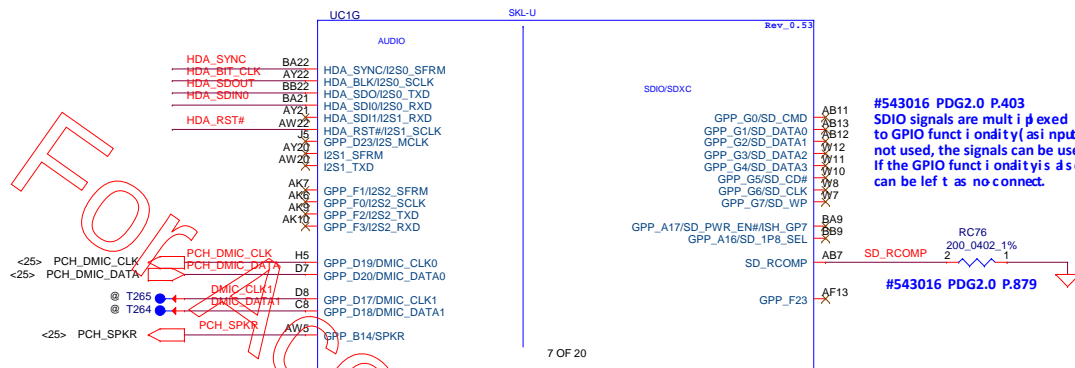


HDA_SDO / I2S_TXD0 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)
Flash Descriptor Security Override
0 = Enable security measures defined in the Flash Descriptor.
1 = Disable Flash Descriptor Security (override). This strap should only be asserted high using external pull-up in manufacturing/debug environments ONLY.

SPKR / GPP_B14 (Internal Pull Down):
(Sampled: Rising edge of PCH_PWROK)

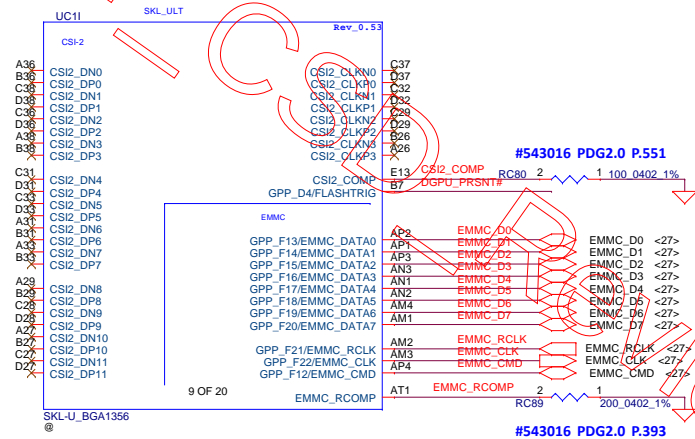
TOP Swap Override
0 = Disable TOP Swap mode.
1 = Enable TOP Swap Mode.

Intel HD Audio link capabilities
> Two SDI signals to support two external codecs.
> Drivers variable frequency (5MHz to 24MHz) BCLK to support:
-- SDO double pumped up to 48 Mb/s
-- SDI's single pumped up to 24 Mb/s
> Provides cadence for 44.1 kHz based sample rate output.
> Support 1.5V, 1.8V, and 3.3V modes.



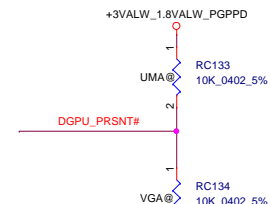
#543016 PDG2.0 P.403
SDIO signals are multiplexed with GPIOs and default to GPIO functionality (as input). If SDIO interfaces are not used, the signals can be used as GPIOs instead. If the GPIO functionality is also not used the signals can be left as no connect.

#543016 PDG2.0 P.879

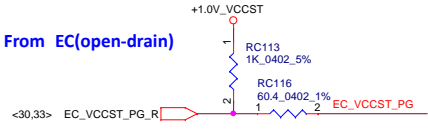
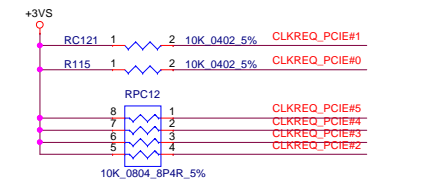
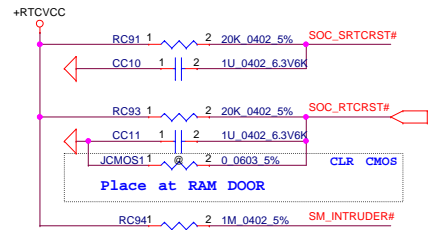


#543016 PDG2.0 P.551

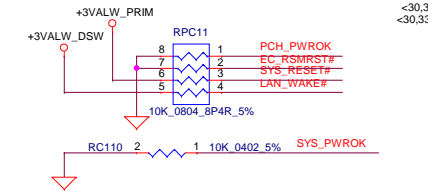
#543016 PDG2.0 P.393



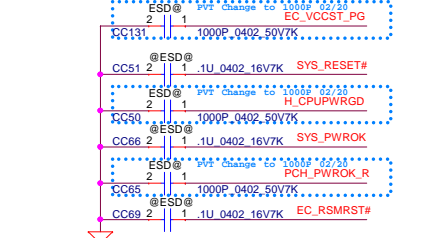
	GPIO67 DGPU_PRSENT#
DIS,Optimus	0
UMA	1



Note for VCCST_PWRGD
 1. 1.0V tolerance
 2. PDG2.0 P.598 Figure43-5 note17: when failure events, VCCST_PWRGD and PCH_PWROK de-assert at the same time

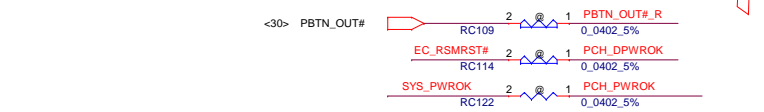
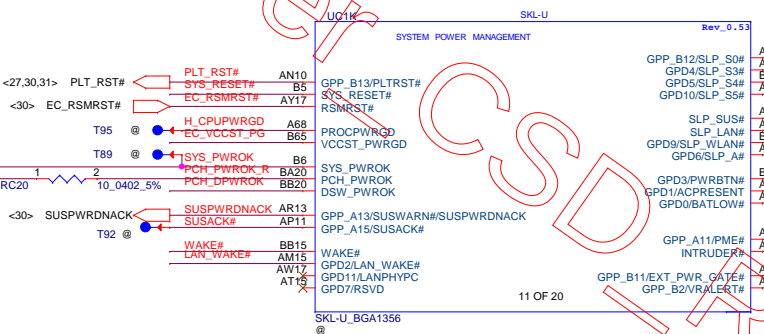
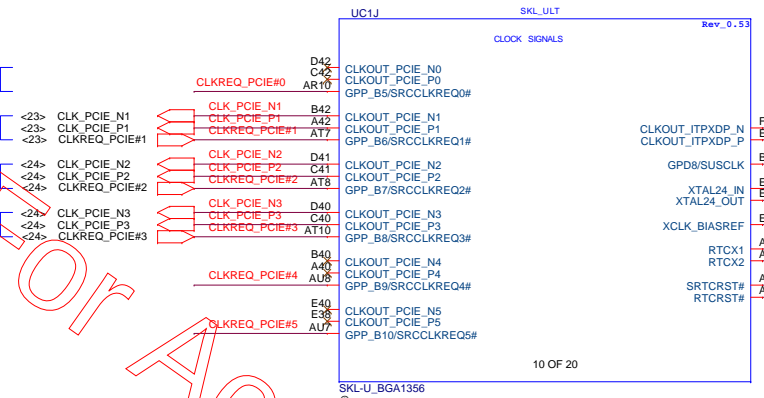


WAKE# (DSX wake event)
 10K pull-up to VccDS_W3_3
 The pull-up is required even if PCIe* interface is not used on the platform

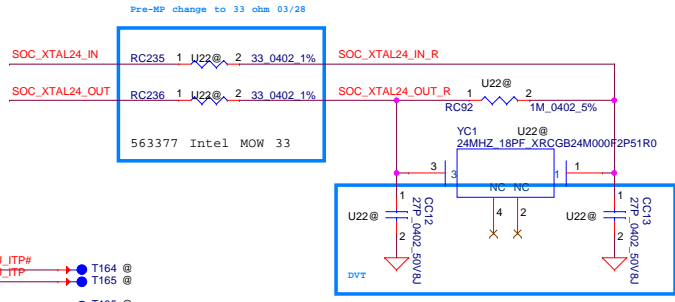
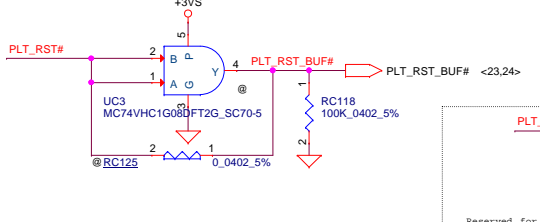


#543016 PDG2.0 P.599
 PROCPWRGD is used only for power sequence debug and is not required to be connected to anything on the platform

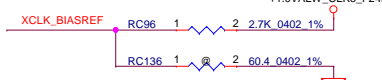
DIS
GLAN
WLAN
mSATA/SSD



PCH PLTRST Buffer

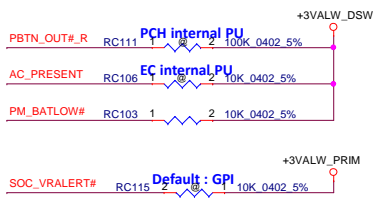
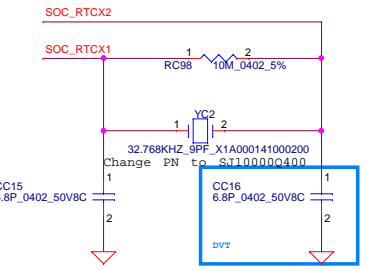


Follow 2014MOW48
 Skylake U PU 2.7k ohm to 1V
 Cannonlake U PD 60.4 ohm



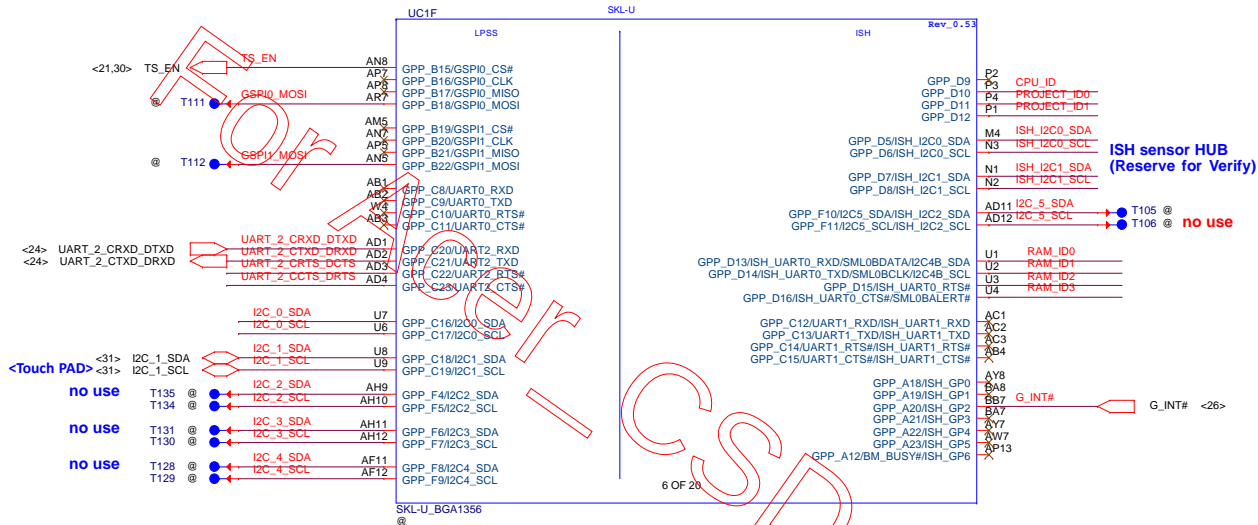
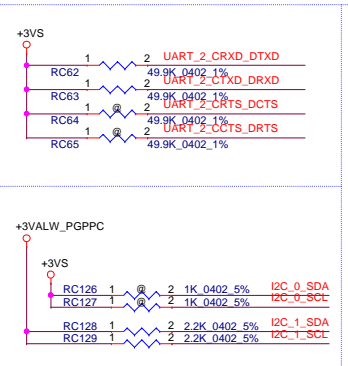
XCLK_BIASREF
 T:50ohm S:12/15 L:1000 Via:2

2014MOW48:
 Skylake-U use 24M 50 ohm ESR
 Cannonlake U use 38.4M 30 ohm ESR



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				SKL-U(5/12)CLK,GPIO	
				Size	
				Custom	
				Document Number	
				CSV01 M/B LA-E891P	
				Rev 1A	
				Date: Monday, June 12, 2017	
				Sheet 11 of 46	

Compal Electronics, Inc.
SKL-U(S/12)CLK,GPIO
 CSV01 M/B LA-E891P
 Monday, June 12, 2017 | Sheet 11 of 46



Functional Strap Definitions

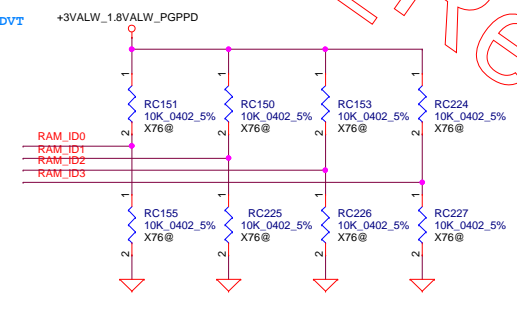
GSPI0_MOSI /GPP_B18 (Internal Pull Down):
(Rising edge of PCH_PWROK)
No Reboot

*0 = Disable No Reboot mode. --> AAX05 Use
1 = Enable No Reboot Mode. (PCH will disable the TCO Timer system reboot feature). This function is useful when running ITP/XDP.

GSPI1_MOSI / GPP_B22 (Internal Pull Down):
(Rising edge of PCH_PWROK)

Boot BIOS Strap Bit
*0 = SPI Mode --> AAX05 Use
1 = LPC Mode

Memory Down Strap

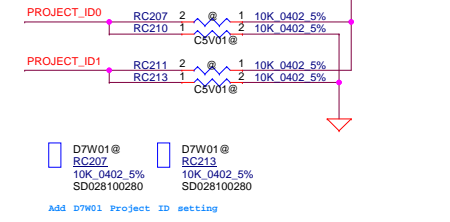


ZZZ	Hynix4GB
X76M01@	X76731BOL01
ZZZ	Samsung4GB
X76M02@	X76731BOL02
ZZZ	Micron4GB
X76M03@	X76731BOL03

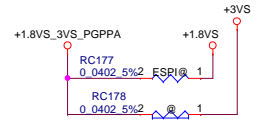
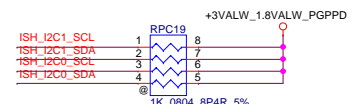
	RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
Hynix 4Gb	0	0	0	0	SA0000A1H20 (\$ IC D4 512M16 H5AN8G6NAFR-UHC FBGA ABOI)
Micron 4Gb	0	0	0	1	SA00009V220 (\$ IC D4 512M16 MT40A512M16Y-083E-B ABOI)
Samsung 4Gb	0	0	1	0	SA00009U420 (\$ IC D4 512M16 K4A8G165WB-BCRC FBGA 96P ABO I)
No on board memory	1	1	1	1	

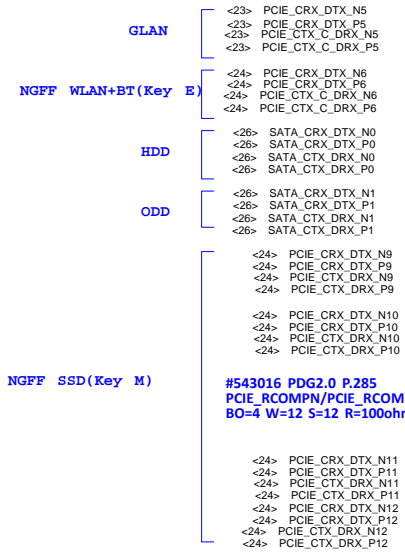
PVT identify U22 , U42 CPU 03/02

	CPU_ID
U22	1
U42	0

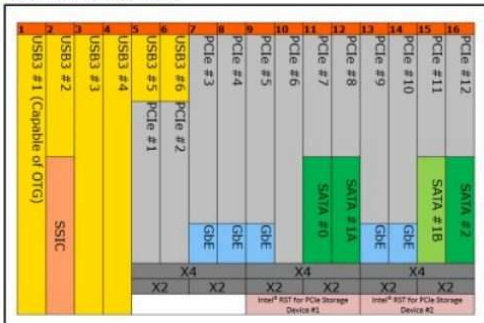


Project ID	Project_ID1 GPP_D12	Project_ID0 GPP_D11
* C5V01	0	0
D7W01	0	1
Reserved	1	0
Reserved	1	1



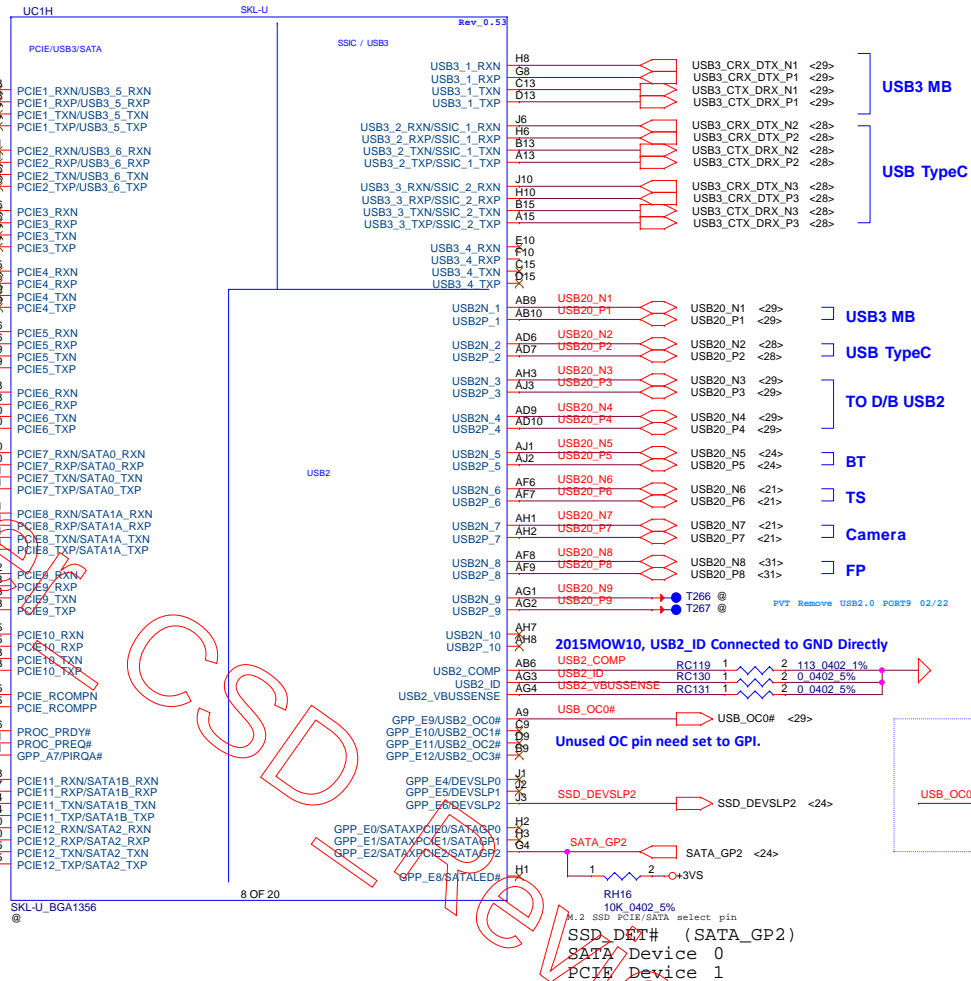


HSIO Multiplexing on PCH-U



PCH-LP Details		PCIe* Controller #1				PCIe* Controller #2				PCIe* Controller #3			
Flex I/O Lane #		5	6	7	8	9	10	11	12	13	14	15	16
PCIe* Lane #		1	2	3	4	5	6	7	8	9	10	11	12
Base-U	1x4	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	1x2+2x1	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x1+1x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
Premium-U	1x4	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	1x2+2x1	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23
	2x1+1x2	RP1	RP3	RP5	RP7	RP9	RP11	RP13	RP15	RP17	RP19	RP21	RP23

vinafix



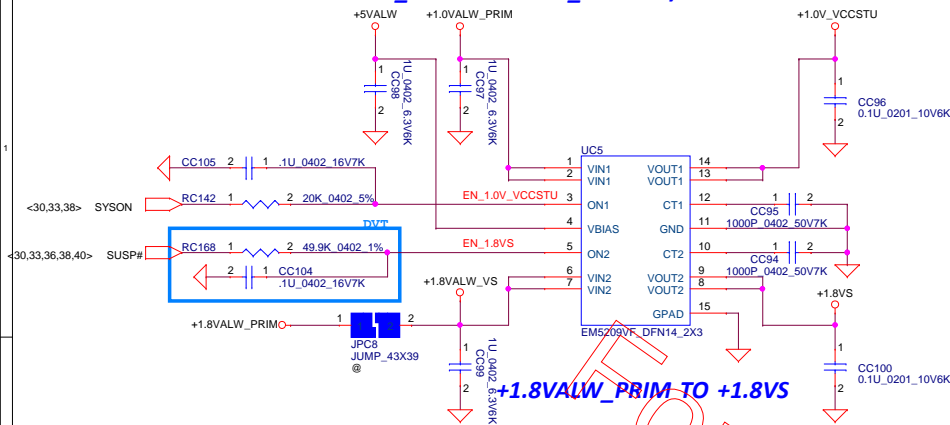
GPIO	DEVICE CONTROL
USB_OC0#	USB2 Port 1
USB_OC1#	NA
USB_OC2#	NA
USB_OC3#	NA
DEVSLP0	NA
DEVSLP1	NA
DEVSLP2	NA
SATA_GP0	NA
SATA_GP1	NA
SATA_GP2	NA

DEVSLP[2:0] Implementation
DEVSLP is a host-controlled hardware signal which enables a SATA host and device to enter an ultra-low interface power state, including the possibility to completely power down host and device PHYs.
The processor provides three SATA DEVSLP signals, DEVSLP[2:0] for SKL U.
• When high DEVSLP requests the SATA device to enter into the DEVSLP power state
• When low DEVSLP requests the SATA device to exit from the DEVSLP power state and transition to active state.

SATA General Purpose (SATAGP[2:0]) Signals
• The processor provides three SATA general purpose input signals SATAGP[2:0] for SKL U. These signals can be configured as interlock switch inputs corresponding to a given SATA port.
• When used as an interlock switch status input on this signal should be driven to 0 to indicate that the switch is closed and to a 1 to indicate that the switch is open.
If mechanical presence switches will not be used on the platform SATAGP[2:0] signals can be configured as GPP_E[2:0] GPIOs signals.

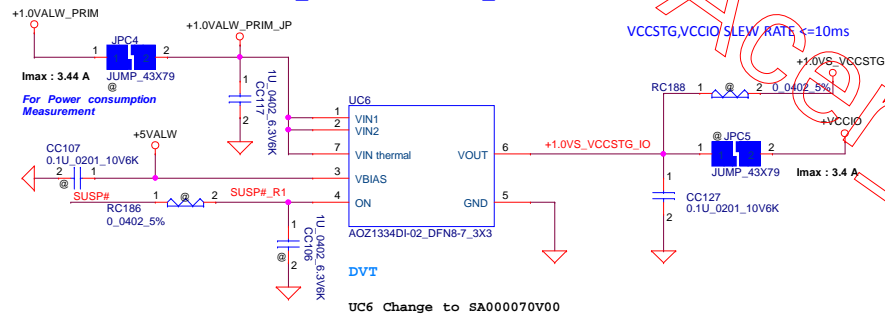
Security Classification		Compal Secret Data		Title	
Issued Date	2016/11/04	Deciphered Date	2018/11/04	Document Number	SKL-U(7/12)PCIe,USB,SATA
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+1.0VALW_PRIM TO +1.0V_VCCSTU / +1.0VCCST

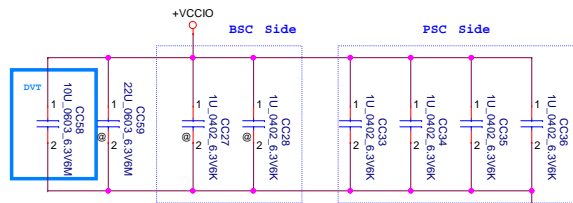


+1.0VALW_PRIM TO +1.0VS_VCCSTG

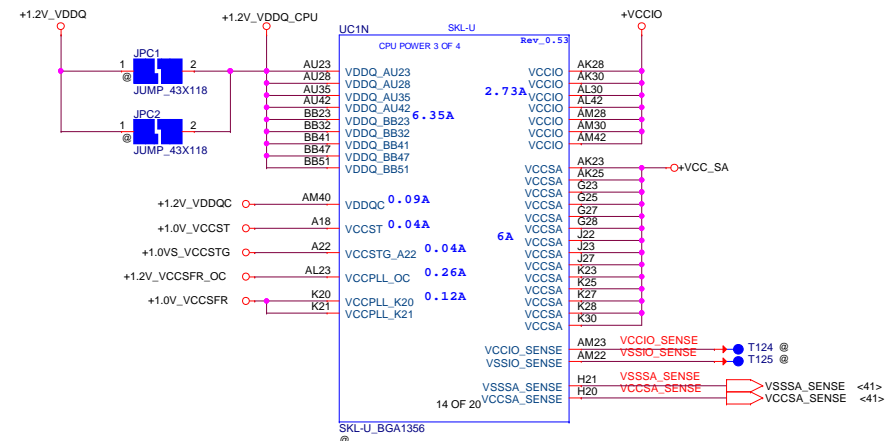
VCCSTG,VCCIO SLEW RATE <=10ms



UC6 Change to SA000070V00



#543016 PDG2.0 P.750
+VCCIO : 4x 1uF 0402



#543016 PDG2.0 P.750
+1.35V_VDDQC : 1x 10uF

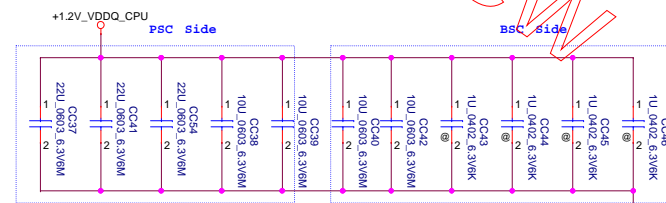
#543016 PDG2.0 P.750
+1.0V_VCCST : 1x 1uF

#543016 PDG2.0 P.750
+1.0V_VCCSFR : 1x 1uF

Reference GND as possible.

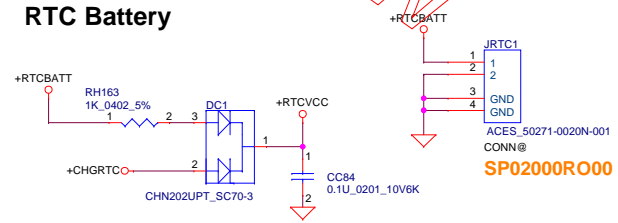
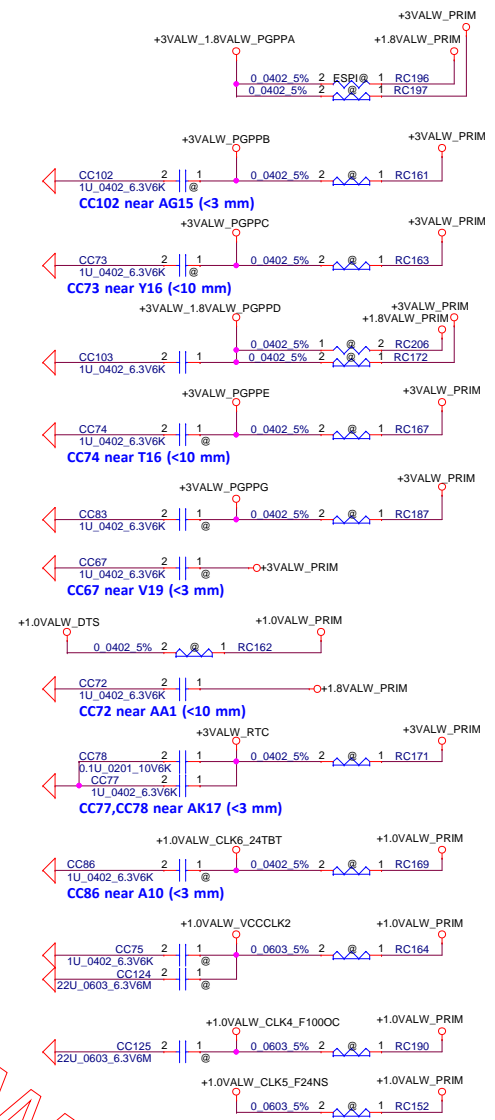
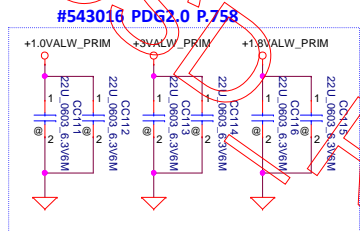
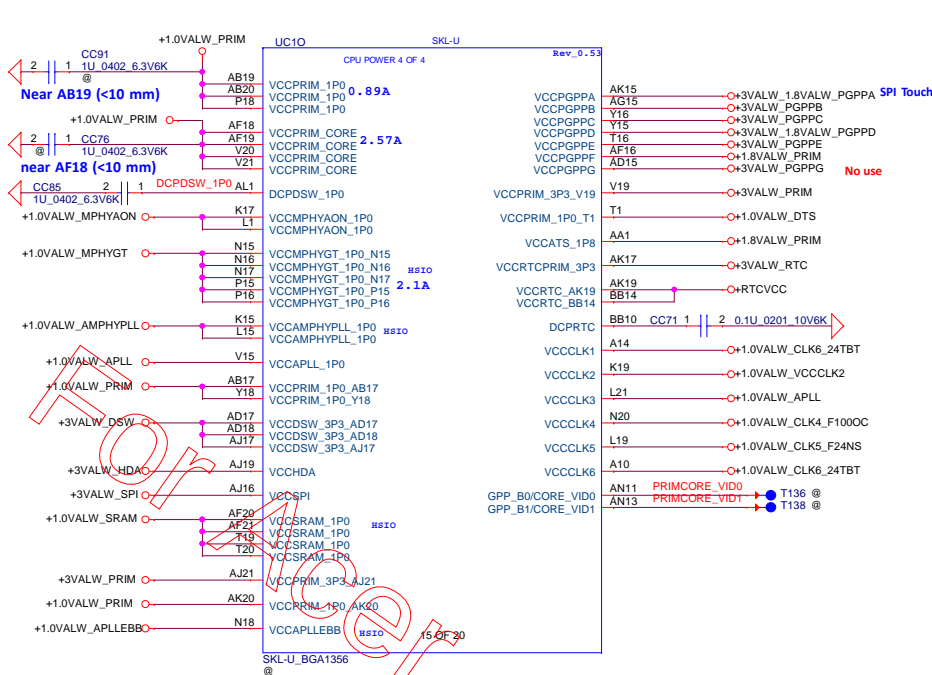
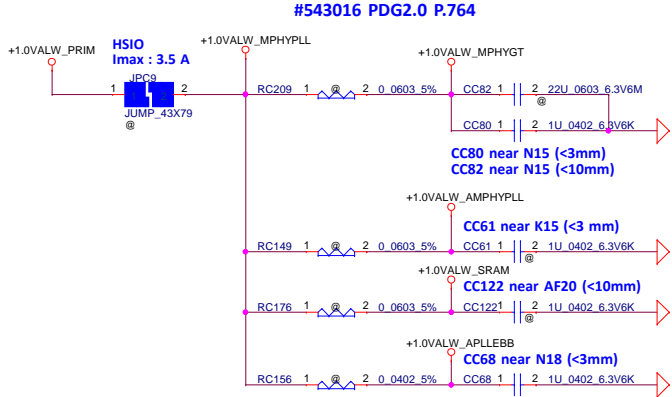
#543016 PDG2.0 P.750
+1.35V_VCCSFR_OC : 1x 1uF

#543016 PDG2.0 P.750
+1.0V_VCCSTG : 1x 1uF (Placeholder)



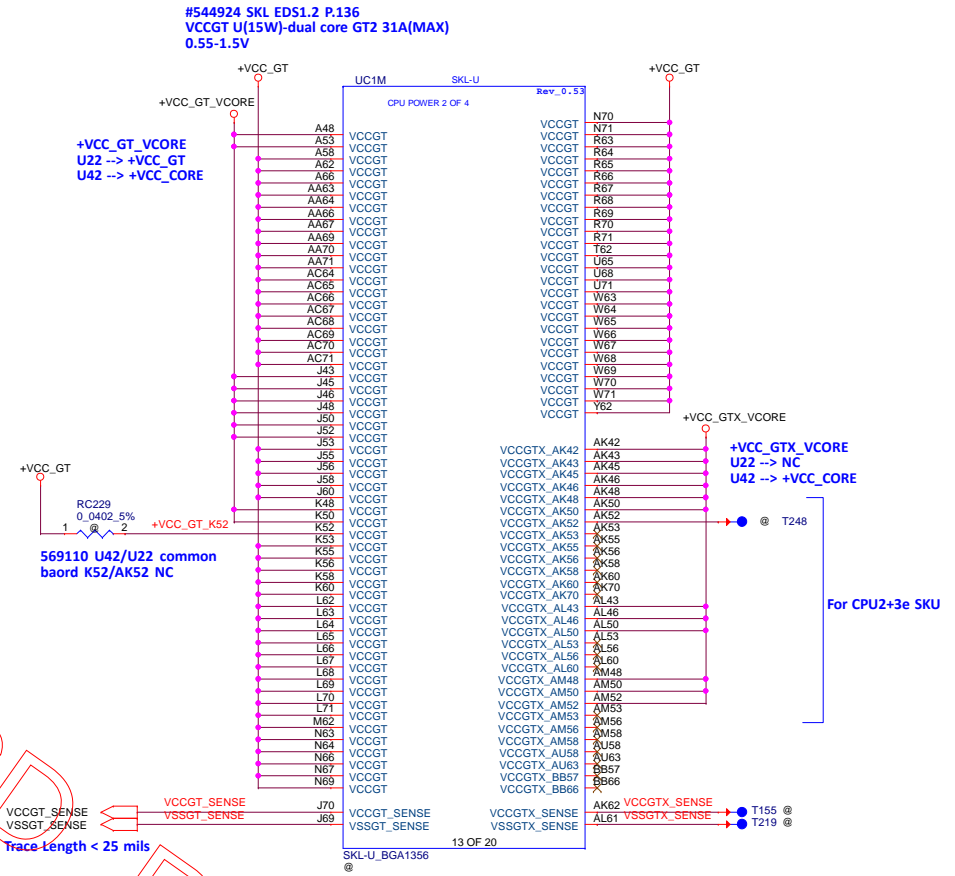
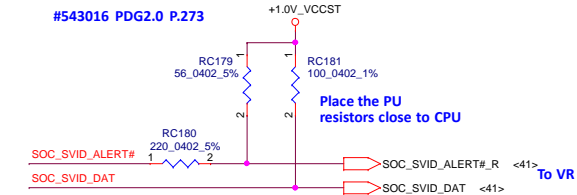
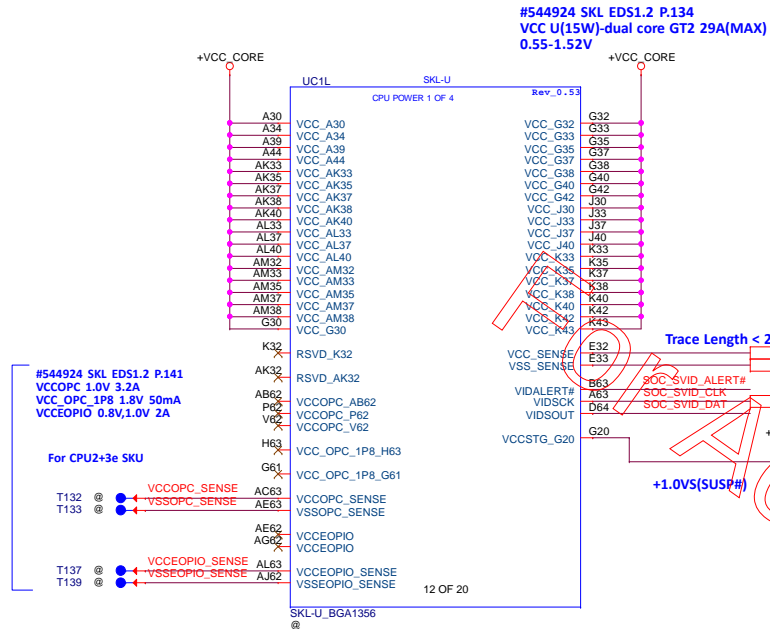
#543016 PDG2.0 P.750
+1.35V_VDDQ_CPU :
4x 10uF 0402
3x 22uF 0603

Security Classification		Compal Secret Data		Title	
Issued Date	2016/11/04	Deciphered Date	2018/11/04	SKL-U(8/12)Power	
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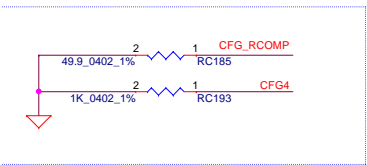
#543016 PDG2.0 P.470
VCCRTC does not exceed 3.2 V.

Power Rail	Voltage
+CHGRTC	3.383V(MAX)
BAT54C(VF)	240 mV
+RTCVCC	3.143V
Result : Pass	

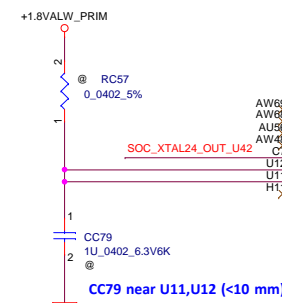
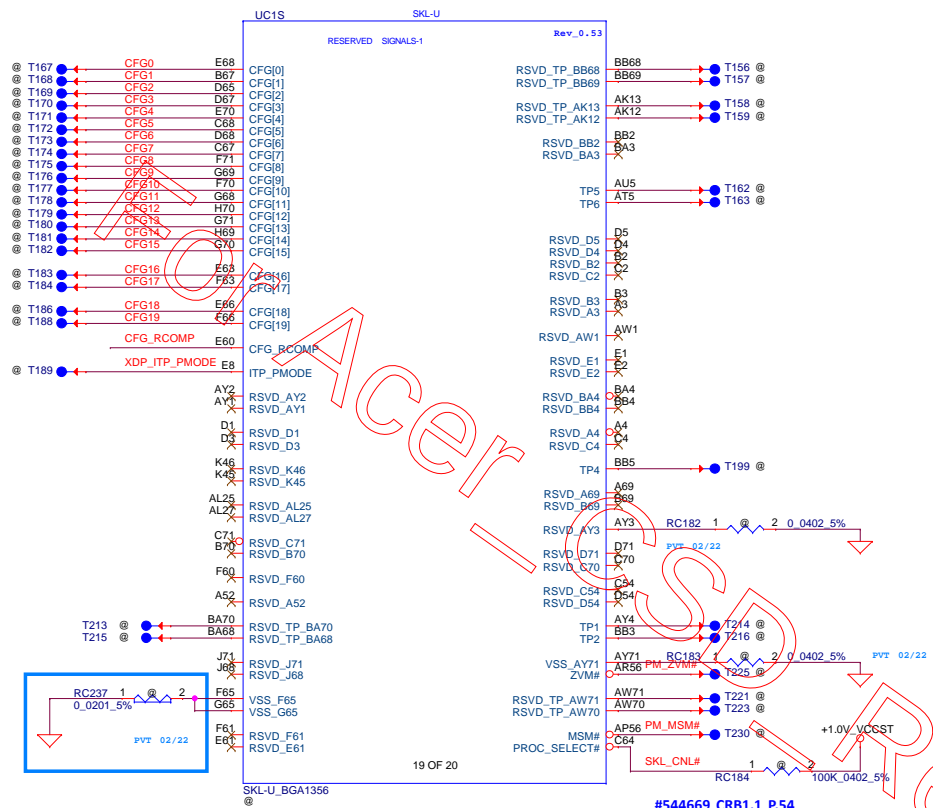


Processor Power Rails

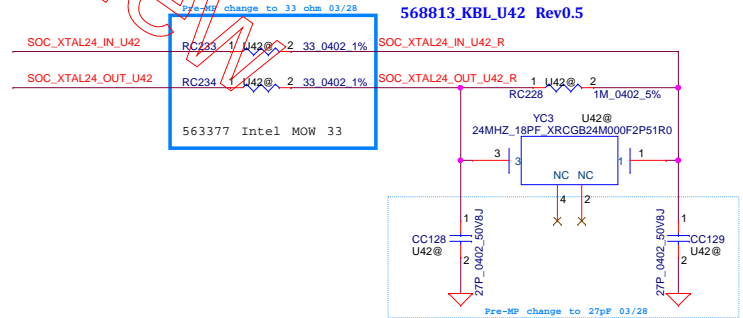
Power Rail	Description	Control
Vcc	Processor IA Cores Power Rail	SVID
VccGT	Processor Graphics Power Rails	SVID
VccGTx	Processor Graphics Extended Power Rail Available only for GT3/GT4 processor SKUs	SVID
VccSA	System Agent Power Rail	SVID/Fixed (SKU dependent)
VccIO	IO Power Rail	Fixed
VccST	Sustain Power Rail	Fixed
VccPLL	Processor PLLs power rail	Fixed
VDDQ	Integrated Memory Controller Power Rail	Fixed (Memory technology dependent)
VccOPC	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VccOPC_1P8	Processor OPC power rail (available only in SKU's with OPC)	Fixed
VccEOPIO	Processor EOPIO power rail (available only in SKU's with OPC)	Fixed

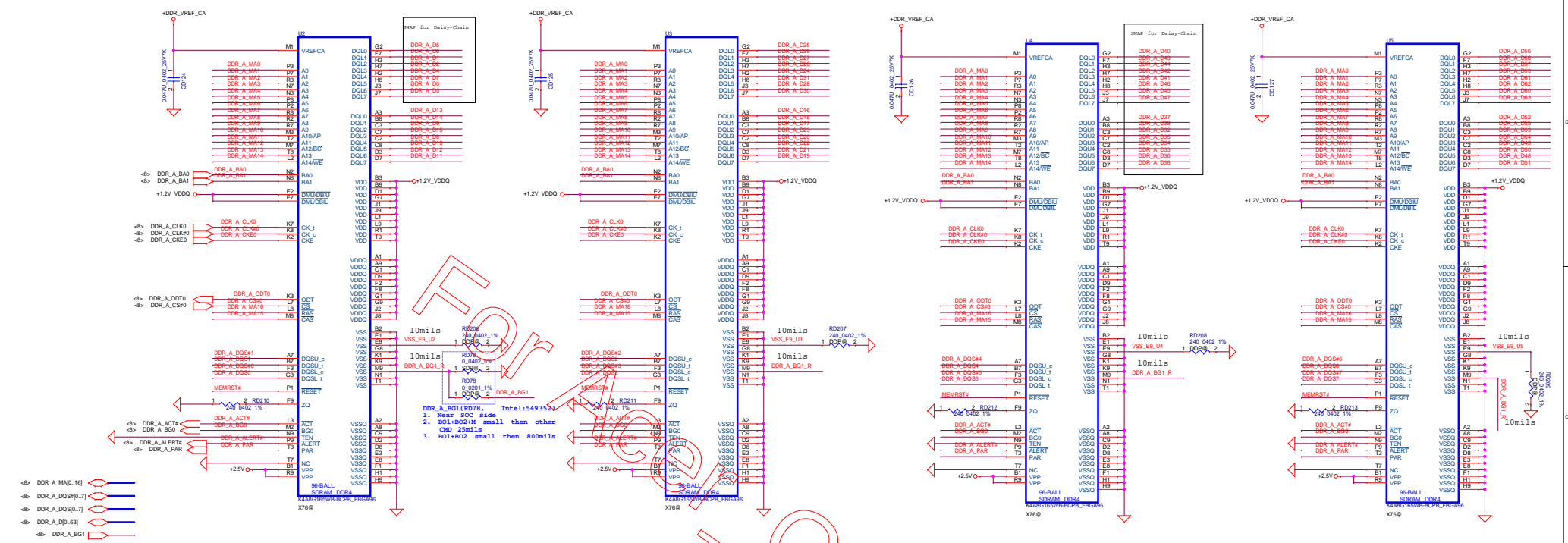


Display Port Presence Strap	
CFG4	1 : Disabled; No Physical Display Port attached to Embedded Display Port 0 : Enabled; An external Display Port device is connected to the Embedded Display Port

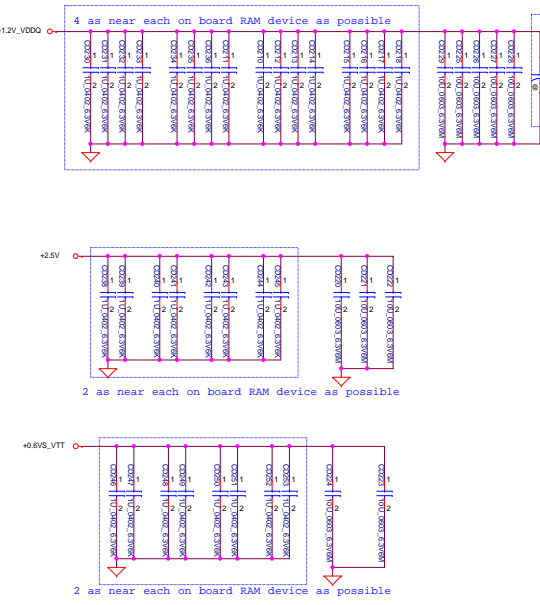
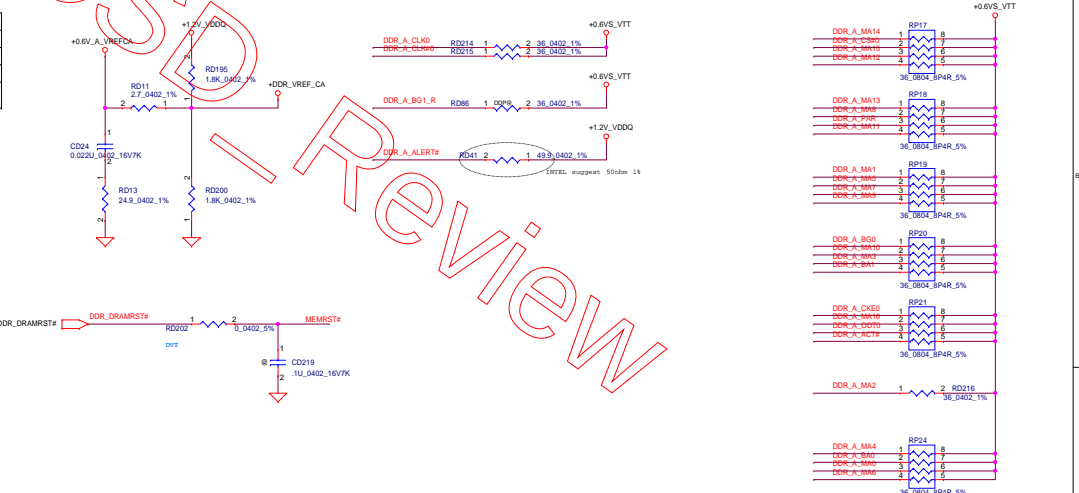


For 2+3e Solution
PM_ZVM#
Zero Voltage Mode: Control Signal to OPC VR, when low OPC VR output is 0V.
PM_MSM#
Minimum Speed Mode: Control signal to VccOPIO VR (connected only in 2 VR solution for OPC).





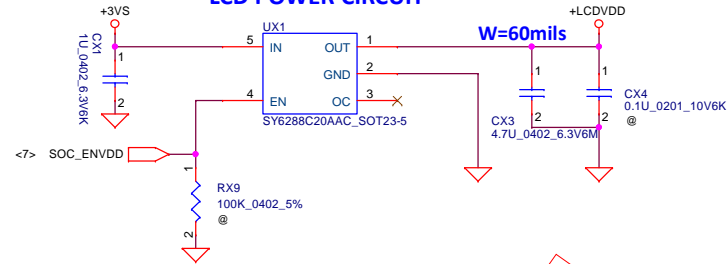
DDR4 mapping	SDP	DDP
E9	VSS	U2Q
M9	VSS	BG1
T7	NC	VSS
RCOMP(0)	200_1%	121_1%



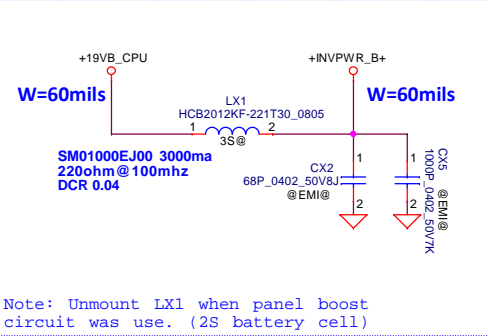
RAM_ID3	RAM_ID2	*RAM_ID1	*RAM_ID0	PartNumber - Description
0	0	0	0	SA0000A1H20 (5 IC D4 512M16 HSANBGNFRA-UHC FBGA ABO1)
0	0	0	1	SA0000V220 (5 IC D4 512M16 MT40A512M16V-083E-B ABO1)
0	0	1	0	SA0000U420 (5 IC D4 512M16 KAAB6165W-BRCR FBGA 96P ABO1)
1	1	1	1	No on board memory

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Title			
DDR4 DIMMB			
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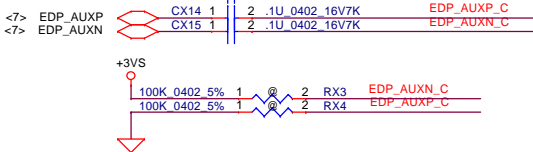
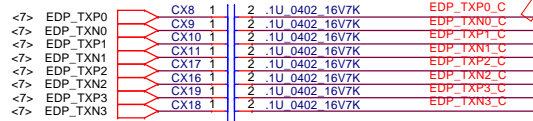
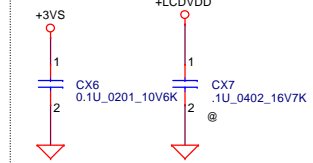
LCD POWER CIRCUIT



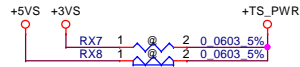
LX1.1 change to +19VB_CPU for layout routing request



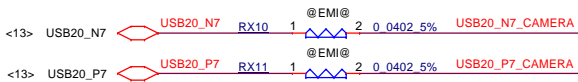
Place closed to JEDP1



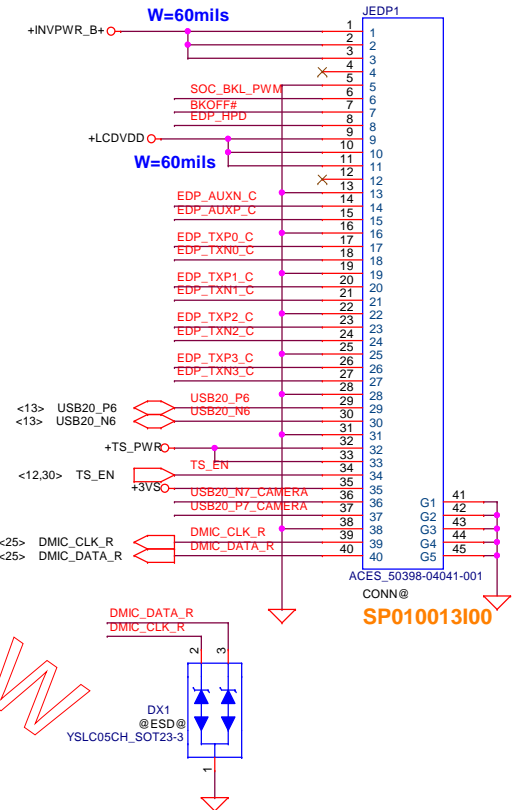
Touch Screen



Camera



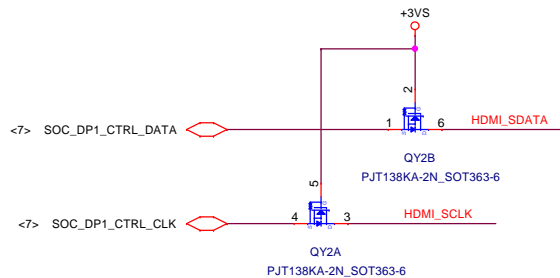
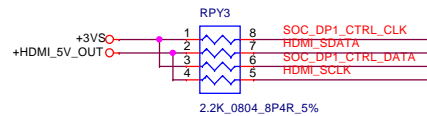
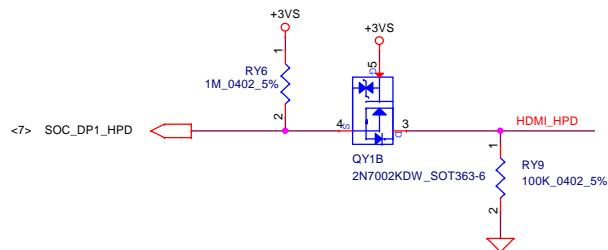
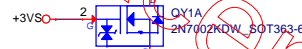
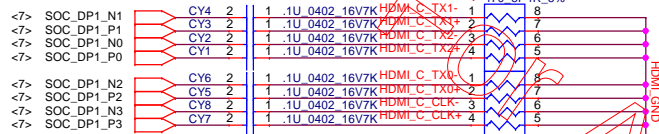
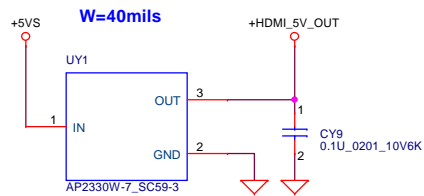
LED PANEL Conn.



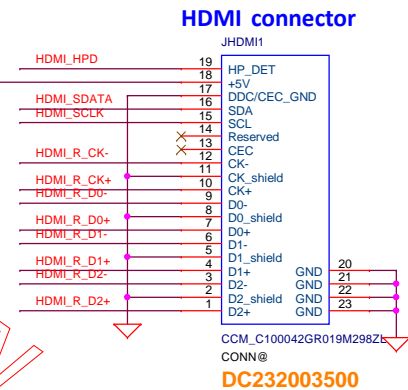
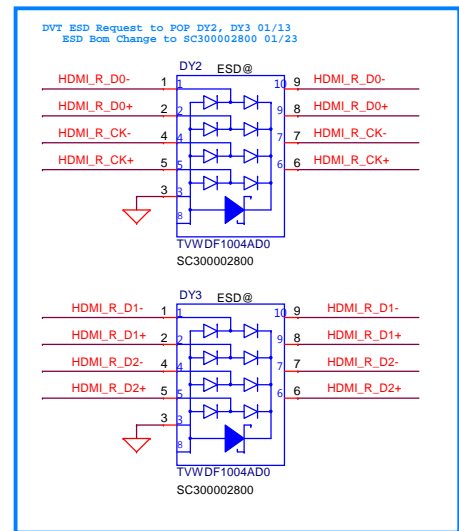
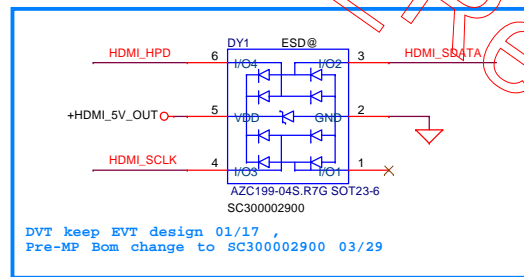
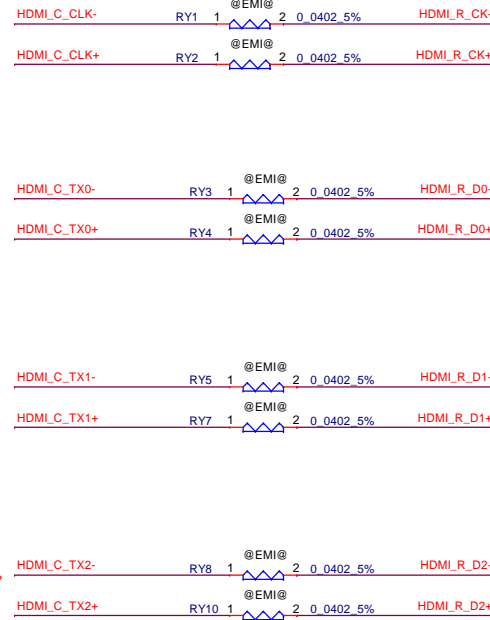
Touch Screen

For Camera

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Issued Date	2016/11/04	Deciphered Date	2018/11/04	Title	
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Size	Document Number	Rev		1A	
Custom	C5V01 M/B 1A-E891P	Date:		Monday, June 12, 2017	
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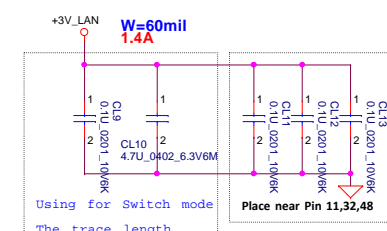
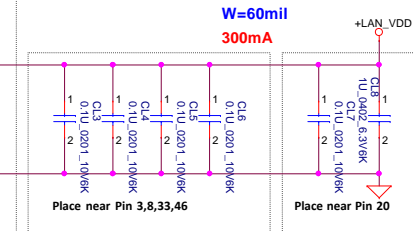
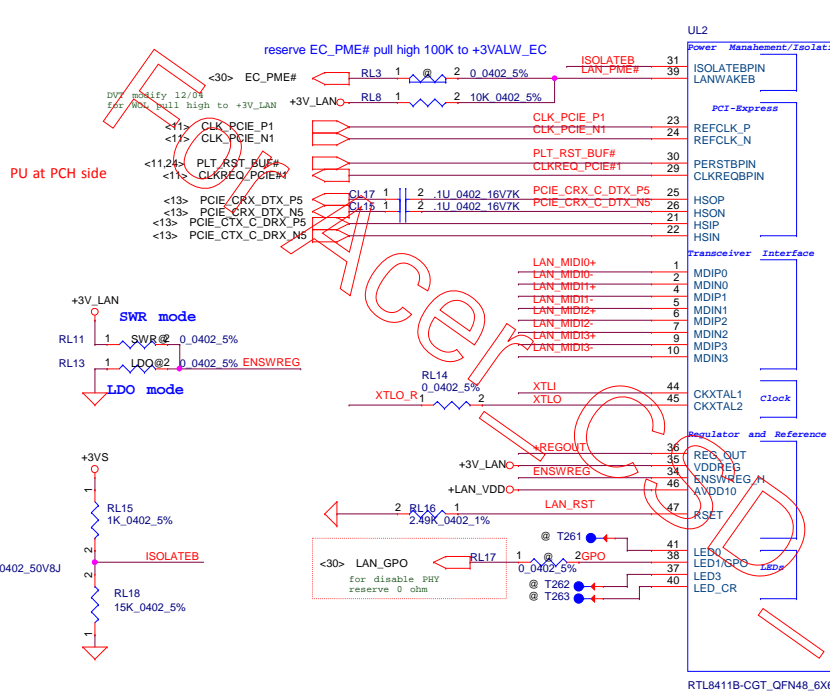
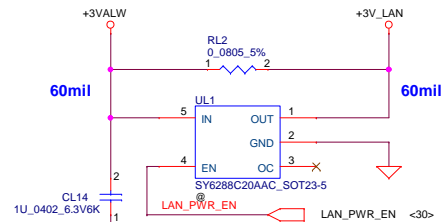


Intel spec Ron/Cout : 3ohm/10pF.
SB000016K00, S TR PJT138KA 2N SOT363-6

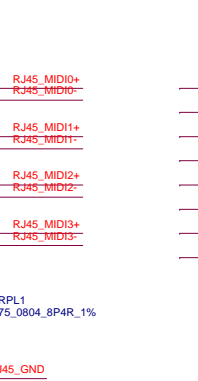
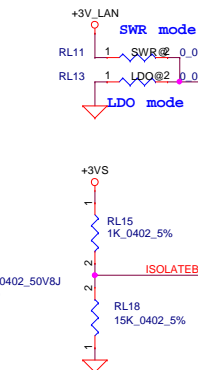


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Size	Document Number	Rev		1A	
Custom	C5V01 M/B LA-E891P	Date:		Monday, June 12, 2017	
Sheet		22		of 46	

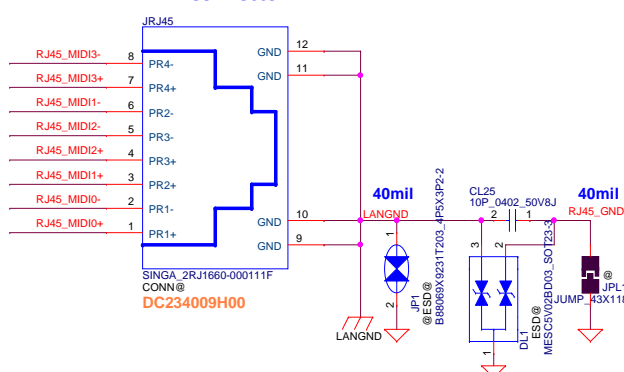
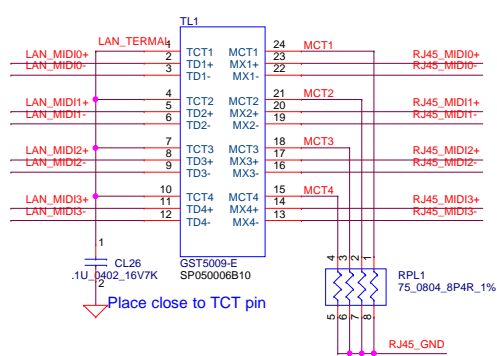
LAN-RTL8411B



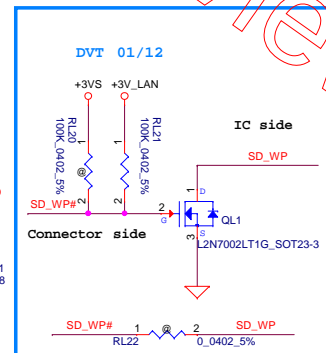
PU at PCH side



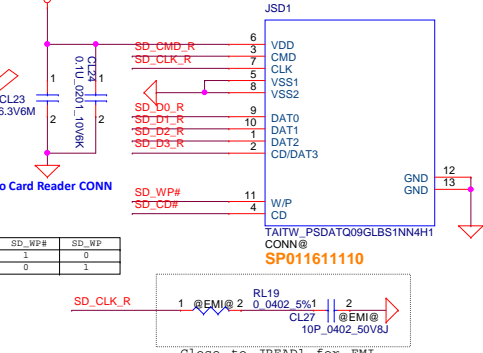
LAN Connector



SD Write protect inverter circuit



Card Reader Connector

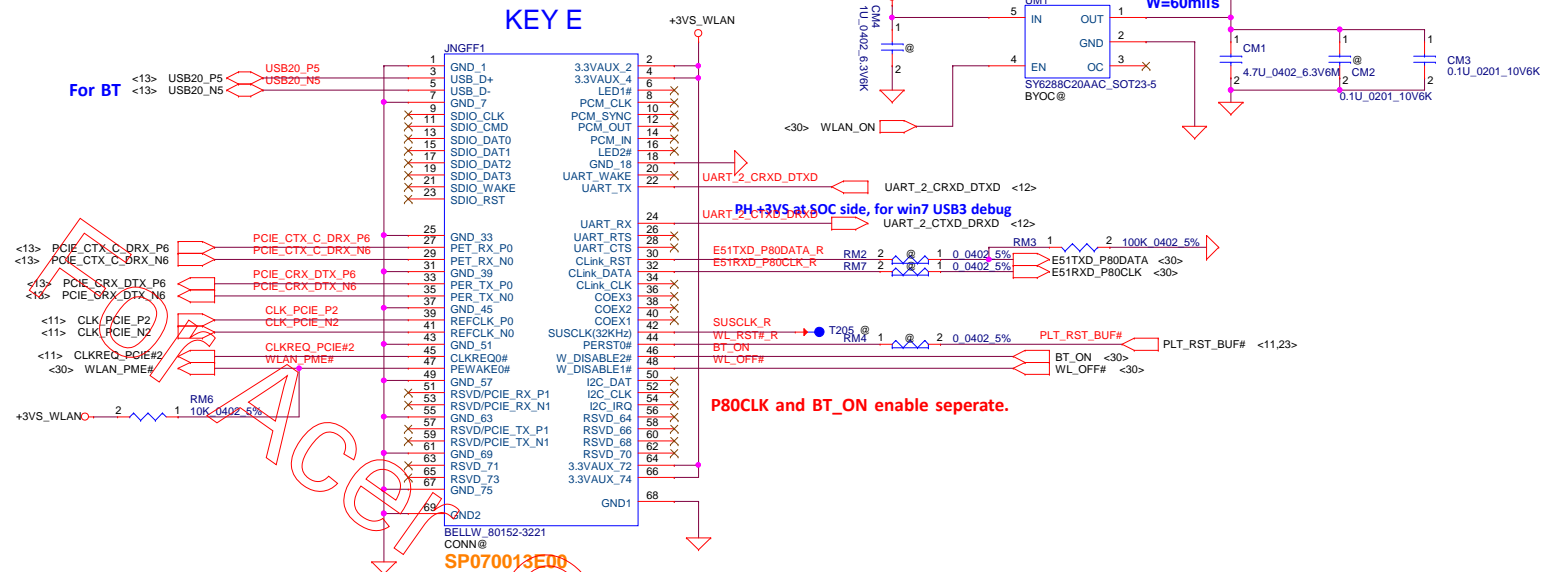


	Protect cotact	Card contact
Write protect (Lock)	Write Enable (Unlock)	
Card Uninsert	Open	Open
Card insert	Open	Close

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								2018/11/04			
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Title				LAN RTL8411B				Rev			
Size				Document Number				1A			
Customer				C5V01 MB LA-E891P							
Date				Monday, June 12, 2017				Sheet 23 of 46			

Wireless LAN

NGFF WL+BT (KEY E)



mSATA/SSD

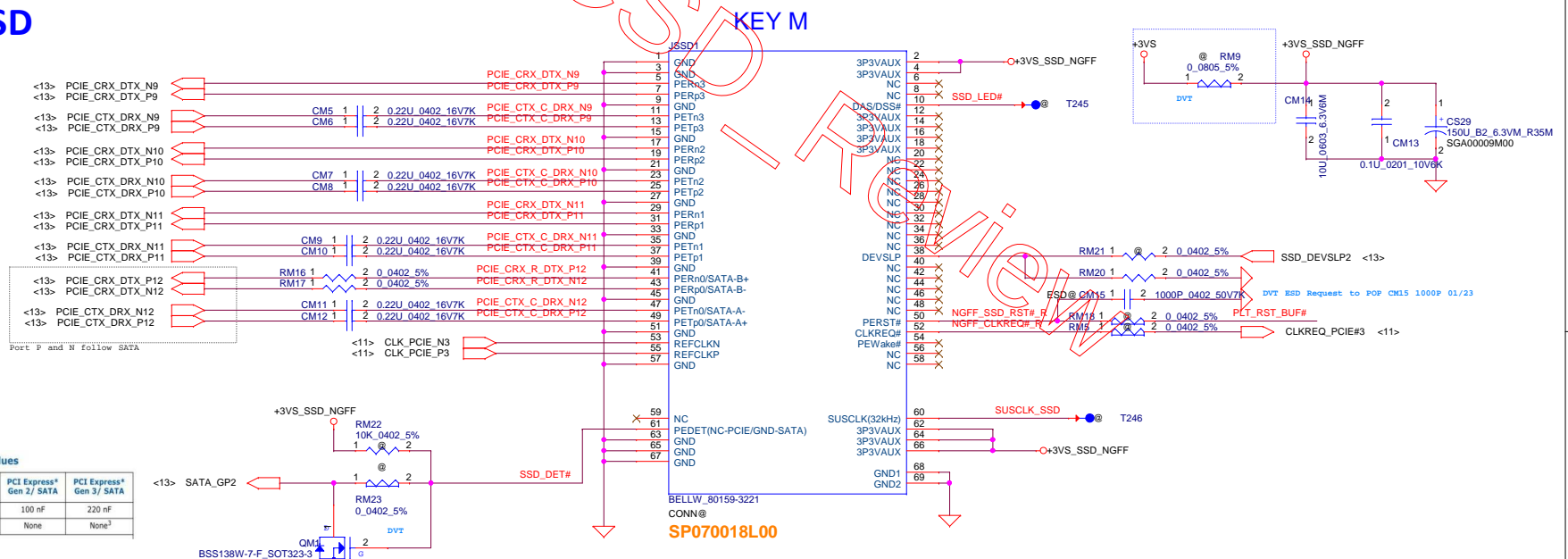


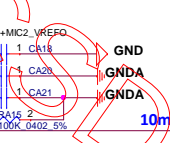
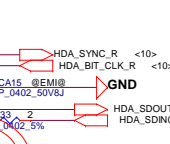
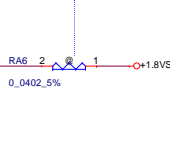
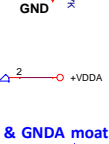
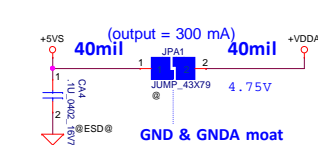
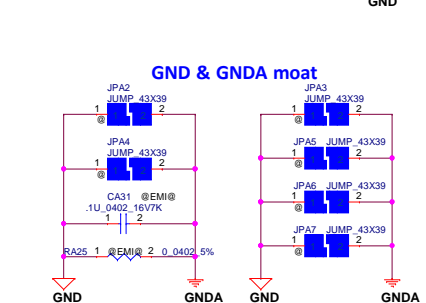
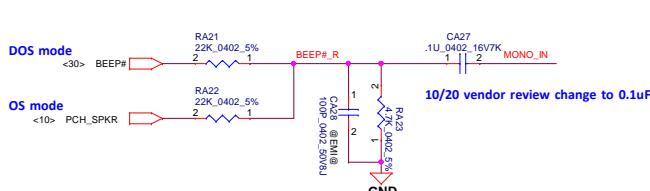
Table 35-7. SATA / PCI Express* Gen 2 and Gen 3 Capacitor Values

Condition	PCI Express* Gen 2 Only	PCI Express* Gen 3 Only	SATA Only	PCI Express* Gen 2/ SATA	PCI Express* Gen 3/ SATA
Processor Tx	100 nF	220 nF	10 nF	100 nF	220 nF
Processor Rx	None	None	10 nF ²	None	None ³

```
SSD_DET# (SATA_GP0)
SATA Device 0
PCIE Device 1
```

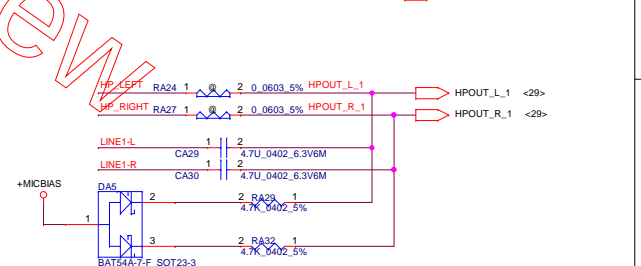
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Issued Date	2016/11/04	Deciphered Date	2018/11/04	Title		
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				Size	Document Number	Rev
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Date:	Monday, June 12, 2017		Sheet	24	of	46

SM01000EJ00 3000mA_220ohm@100mhz DCR 0.04

[illegible]

Timing diagram for DMIC signals. The diagram shows two input signals, PCH_DMIC_DATA and PCH_DMIC_CLK, both with a period of 33.04025ns. These are connected to DMIC_DATA and DMIC_CLK_R. DMIC_DATA is also connected to DMIC_DATA_R and DMIC_CLK_R is connected to DMIC_CLK_R. The diagram includes a blue dashed box labeled "DVT EMI request change 0ohm to Head" containing a component "BLM15P2245N1D" and a pin "SM01000NY00". Other components shown are RA36, RA35, and RA34.

The schematic diagram illustrates the voltage reference circuit for the MIC2158. It features a voltage divider formed by two 2.2K resistors, RA19 and RA20, connected in series between the +MIC2_VREFO input and ground. The midpoint of this divider is connected to the SLEEVE and RING2 pins of the MIC2158. The SLEEVE pin is also connected to a 29-pin connector.



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				Sheet	25 of 46

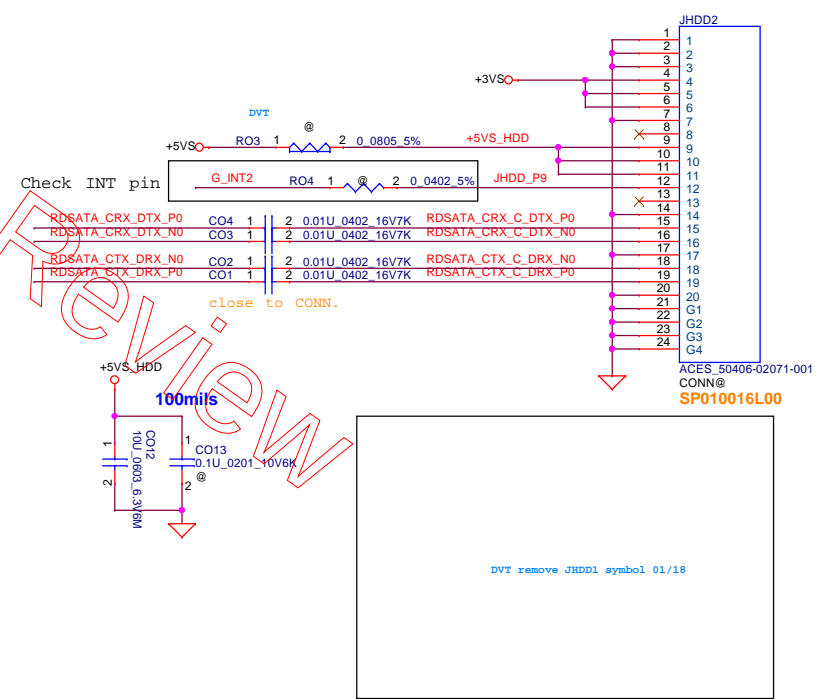
Schematic diagram of the LIS3DH I2C interface circuit. The LIS3DH is connected to a +3VS supply via a 10K pull-up resistor (RZ1) on the BA pin. The CS pin is connected to +3VS. The SCL and SDA pins are connected to a +3VS supply via 10K pull-up resistors (RZ2, RZ3) and to the I2C bus. The INT1 and INT2 pins are connected to a +3VS supply via 10K pull-up resistors (RZ4, RZ5) and to the I2C bus. The RES pin is connected to GND. The GND pin is connected to GND. The I2C bus is connected to a +3VS supply via a 10K pull-up resistor (RZ6). The I2C address is 0x30h.

Schematic diagram of the SATA signal conditioning circuit for the SP01002HK00. The circuit shows the connection of SATA signals (SATA_CTX_DRX_P1, SATA_CTX_DRX_N1, SATA_CRX_DTX_N1, SATA_CRX_C_DTX_P1) to the JODD1 connector. It includes a 5V supply, a 0.0805 5% resistor (RO2), a 10uF 6.3V6W capacitor (CO9), and a 0.1uF 0201 10V6K capacitor (CO10). The output is connected to the JODD1 connector pins 1 through 26, with a GND connection to pin 26. The component values and part numbers are specified: 0.0805 5%, 10uF 6.3V6W, 0.1uF 0201 10V6K, and JODD1. The connector is labeled ACES_50673-0120N-P01 and the component is SP01002HK00.

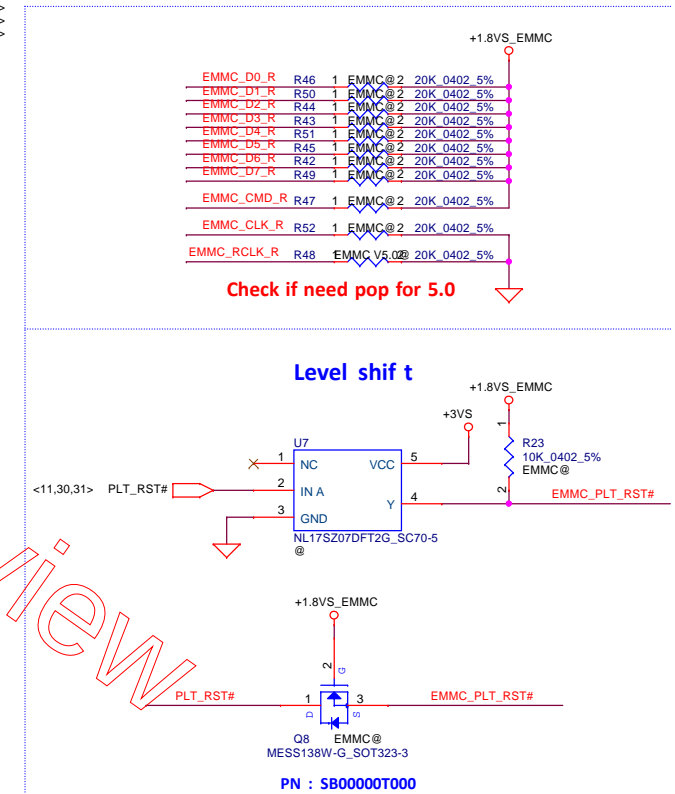
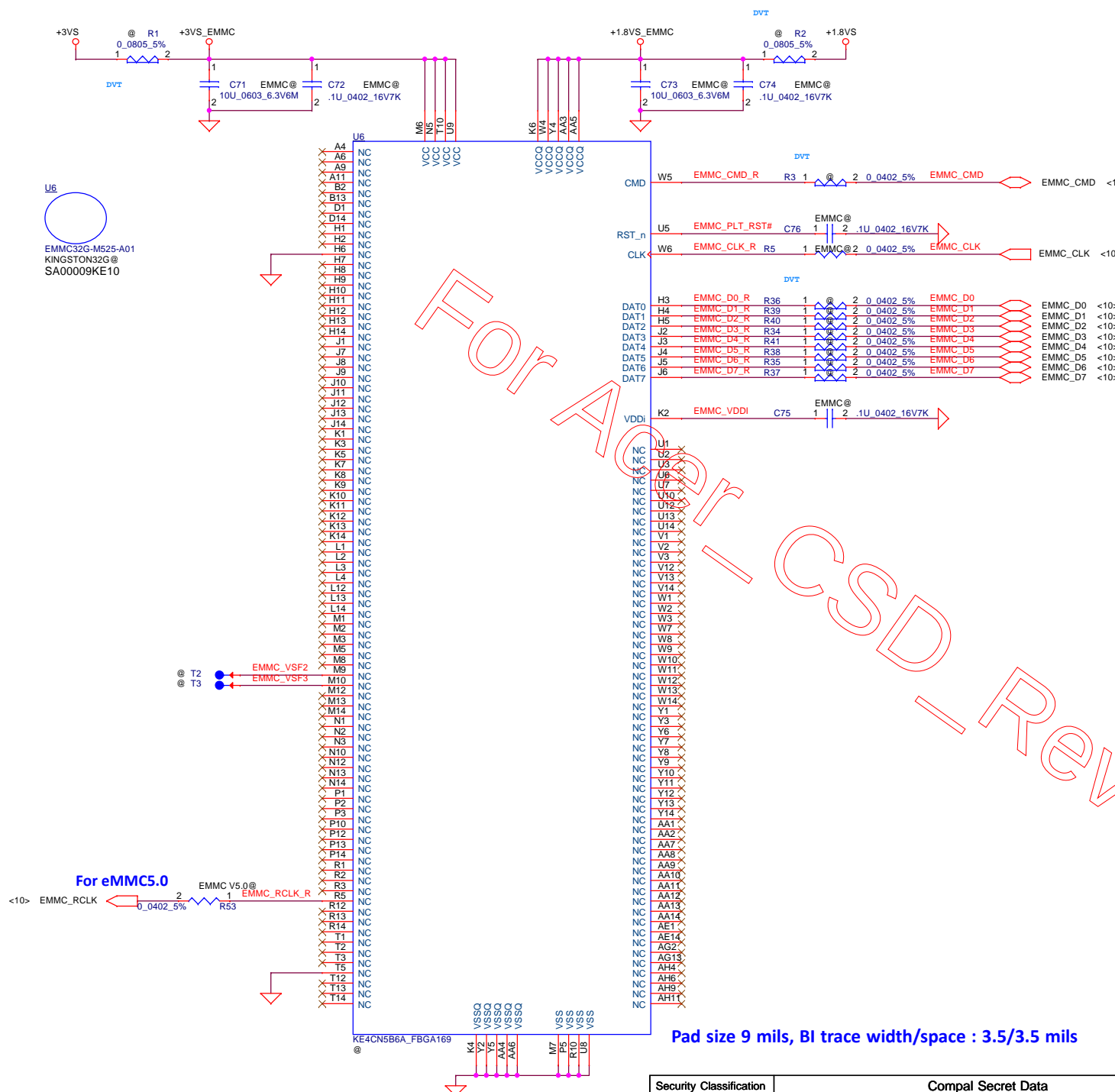
DVT update re-driver EQ setting

The schematic diagram illustrates the DVT update re-driver EQ setting. It features a +3VS supply connected to a network of resistors (RO10-RO22) and capacitors (CO14, CO15). The circuit includes two UO2 components: a PS527CTQFN20GTR2A_TQFN20_4XA and a SN75LVCP601RTJR_A.4_TQFN20_4XA. Various pins are labeled with signals like SATA_CTX_DRX_P0, SATA_CTX_DRX_N0, SATA_CRX_DTX_N0, and SATA_CRX_DTX_P0. A table on the right lists pin parameters and TI components.

PIN	Parameter	TI
1	A_INP	RX1P
2	A_INN	RX1N
3	GND	GND
4	B_OUTIN	TX2N
5	B_OUTP	TX2P
6	REXT	DEW2
7	EN	EN
8	DE	DE2
9	A_DE	DE1
10	VDD	VCC
11	B_INP	RXP
12	B_INN	RXXN
13	B_EQ2	GND
14	A_OUTIN	TX1N
15	A_OUTP	TX1P
16	DEW	DEW1
17	A_EQ2	EQ1
18	A_EQ2	GND
19	B_EQ1	EQ2
20	VDD	VCC



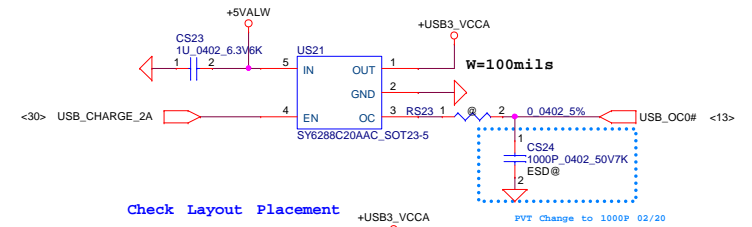
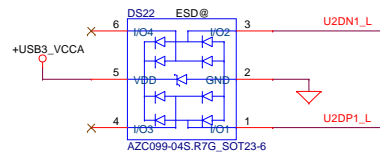
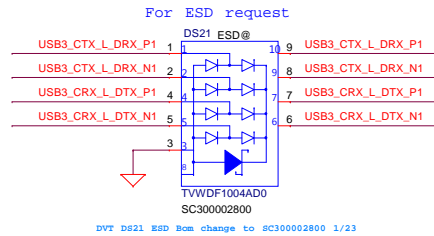
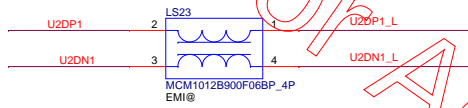
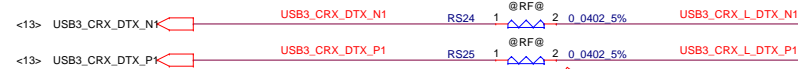
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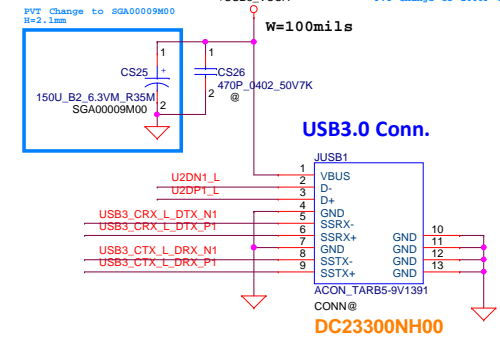
Pad size 9 mils, BI trace width/space : 3.5/3.5 mils

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Size Custom		Document Number		Rev 1A	
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USB3.0 (Port 1)

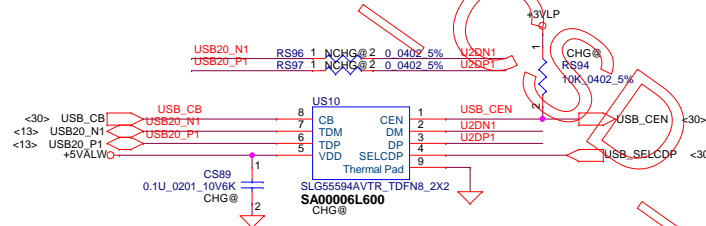


Check Layout Placement

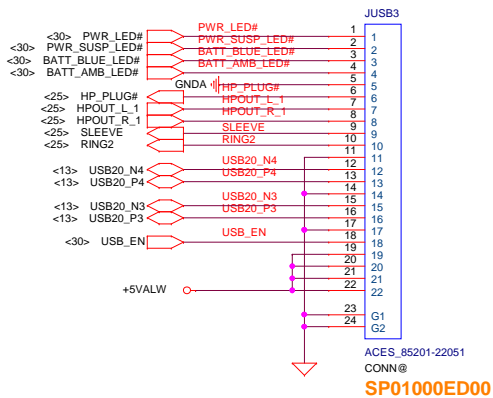


USB Host Charger

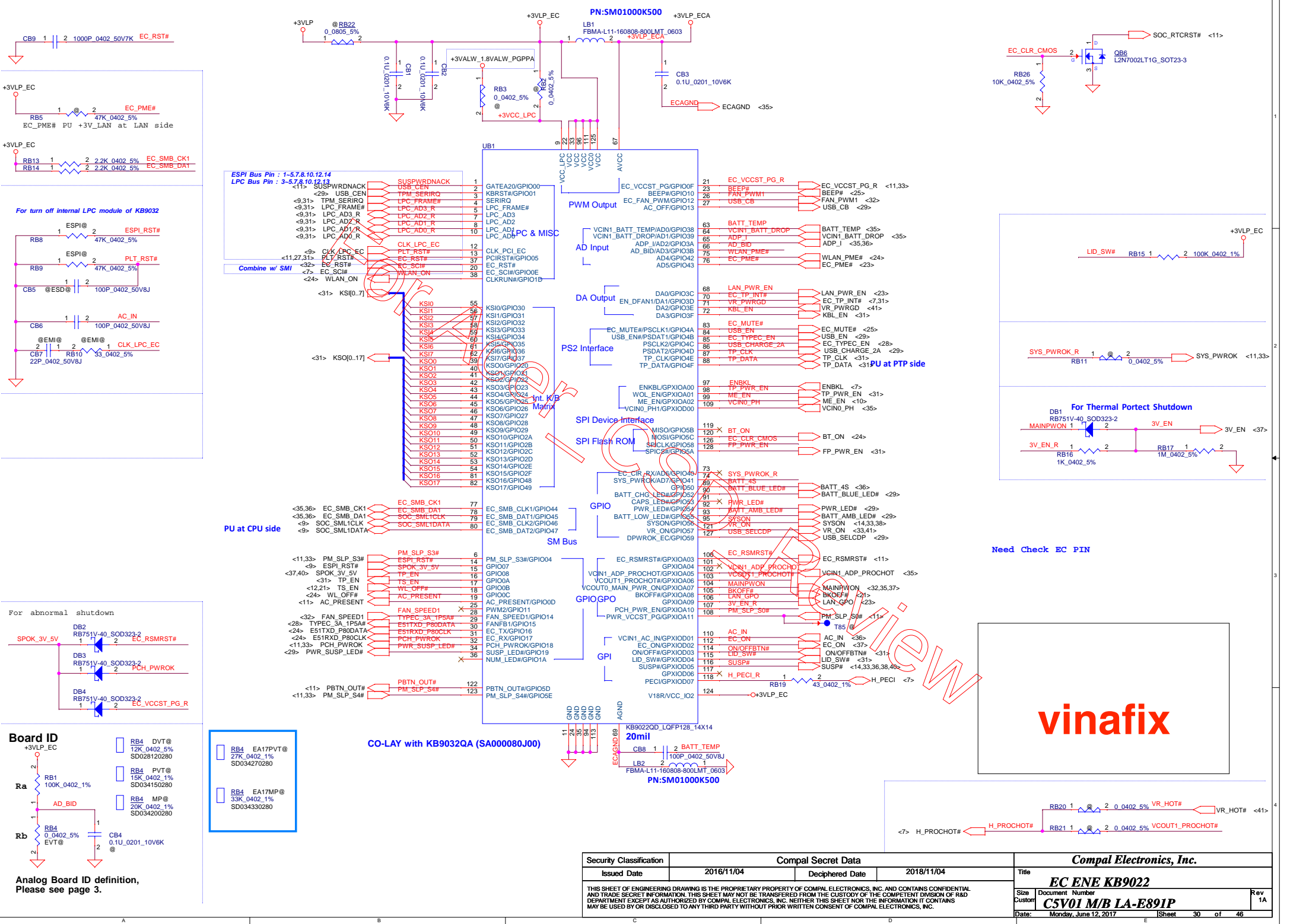
CB	SELCDP	
0	X	DCP(Dedicated Charging Port) autotetect with mouse/keyboard wakeup
1	0	S0 charging with SDP(Standard Downstream Port) only
1	1	S0 charging with CDP(Charging Downstream Port) or SDP only



USB/B (USBx2, AUDIO, LEDx2)



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For turn off internal LPC module of KB9032

For abnormal shutdown

Board ID

Analog Board ID definition, Please see page 3.

ESPI Bus Pin : 1-5,7,8,10,12,14
LPC Bus Pin : 3-5,7,8,10,12,14

PU at CPU side

CO-LAY with KB9032QA (SA000080J00)

PN:SM01000K500

LPC & MISC

DA Output

PS2 Interface

SPI Device Interface

SPI Flash ROM

GPIO

GPIOGPO

GPI

KB9022QD_LQFP128_14X14

PN:SM01000K500

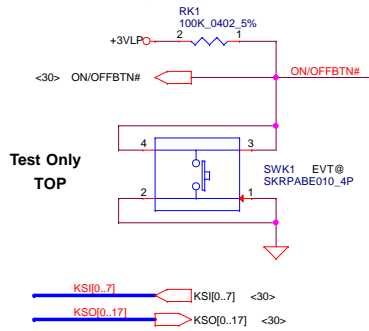
Need Check EC PIN

vinafix

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Size	Custom	Document Number	C5V01 M/B LA-E891P	Rev	1A
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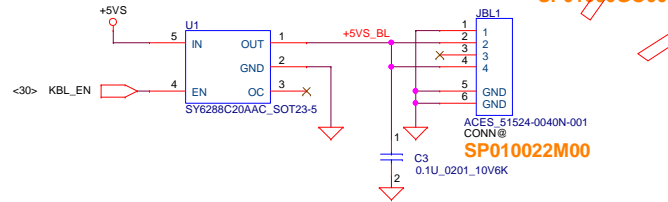
KB Conn.

ON/OFF BTN



Test Only
TOP

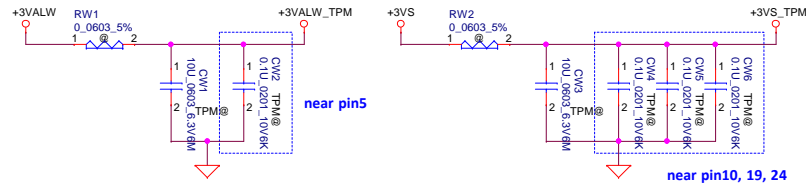
KB BackLight



ACES_86201-2805
CONN@
SP01000G000

ACES_51524-0040N-001
CONN@
SP010022M00

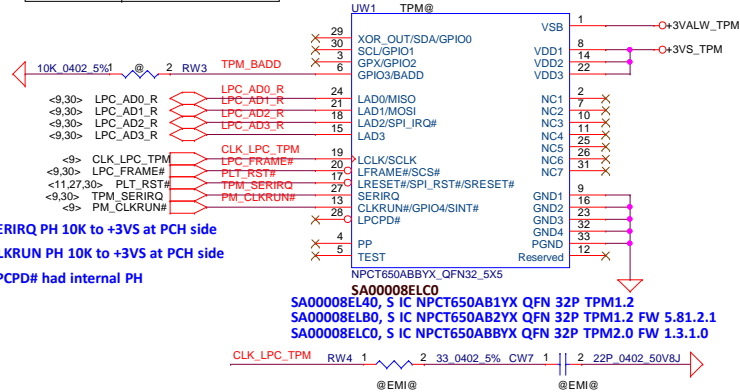
TPM



near pin5

near pin10, 19, 24

BADD	SELECTION
* 1	Aeh(write), Afh(read)



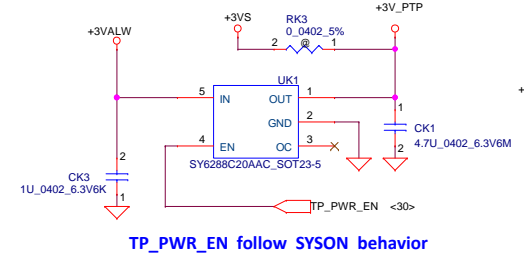
SERIRQ PH 10K to +3VS at PCH side

CLKRUN PH 10K to +3VS at PCH side

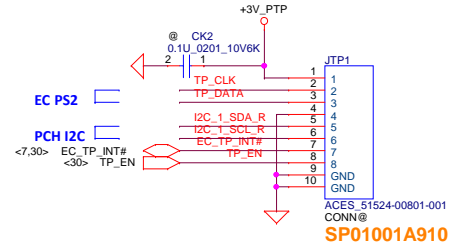
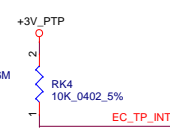
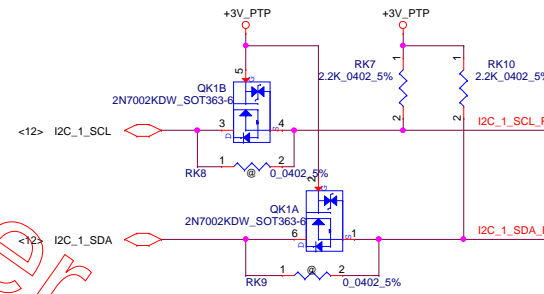
LPCPD# had internal PH

SA00008EL40, S IC NPCT650AB1YX QFN 32P TPM1.2
SA00008ELB0, S IC NPCT650AB2YX QFN 32P TPM1.2 FW 5.81.2.1
SA00008ELC0, S IC NPCT650ABBYX QFN 32P TPM2.0 FW 1.3.1.0

TP/B Conn.



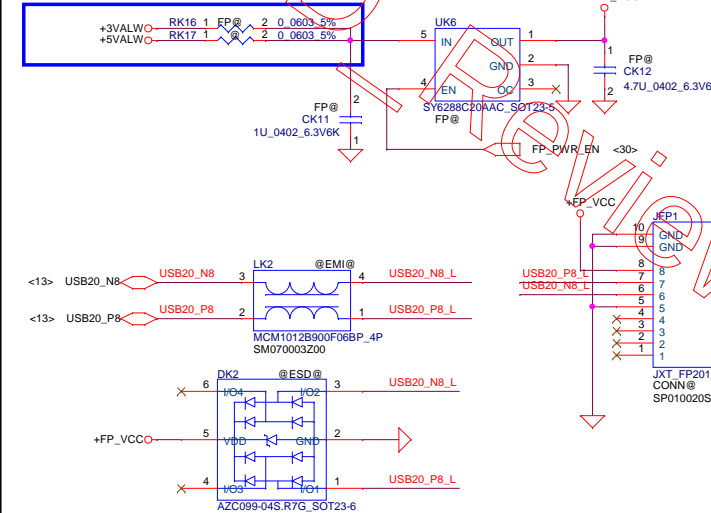
TP_PWR_EN follow SYSON behavior



SP01001A910

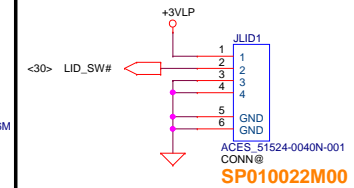
Finger Print

Power Souce Check
EGIS ETU801 +FP_VCC=5V
ELAN SA464K-2200 +FP_VCC=3.3V



Lid Switch

(Hall Effect Switch)

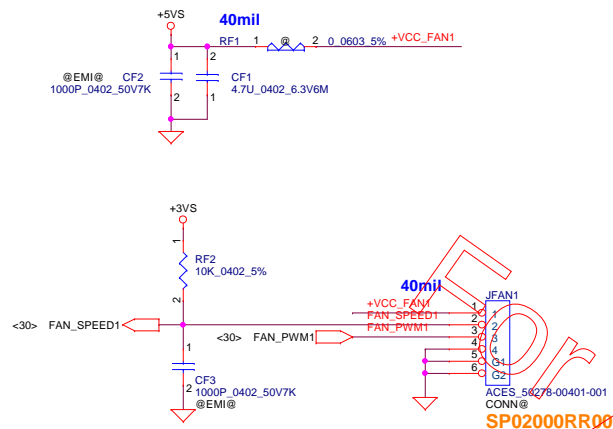


PIN	ETU801	SA464K-2200
1	+FP_VCC (5V)	+FP_VCC (3V)
2	USBP	D+
3	USBN	D-
4	GND	GND
5	NC	NC
6	NC	NC
7	NC	NC
8	NC	NC

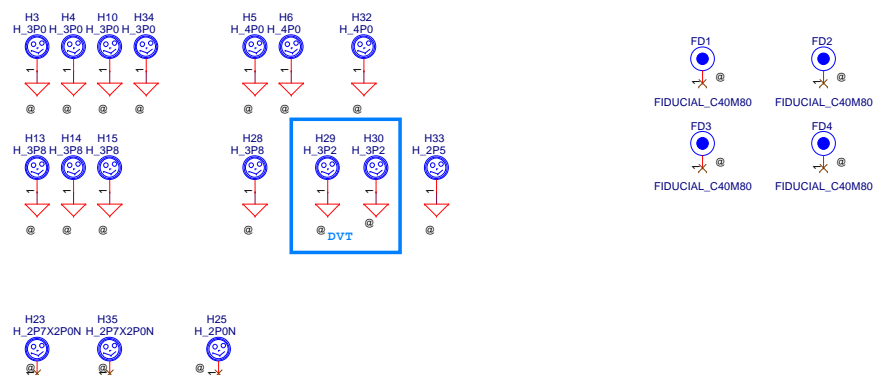
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Compal Electronics, Inc.			
KB & TP & TPM & LID & FP			
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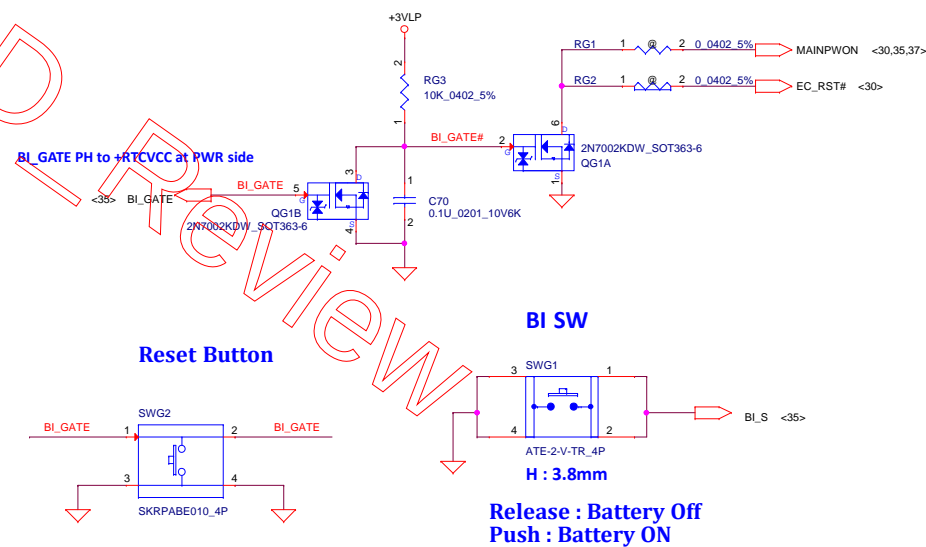
FAN1 Conn



Screw Hole

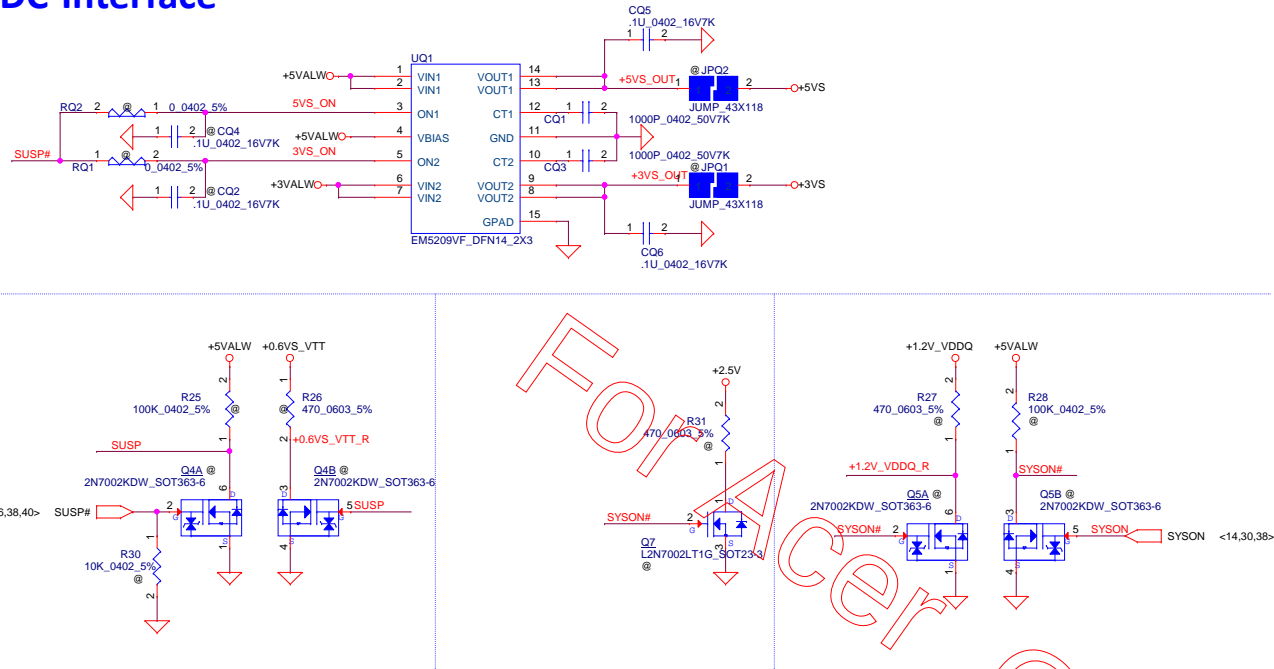


Reset Circuit

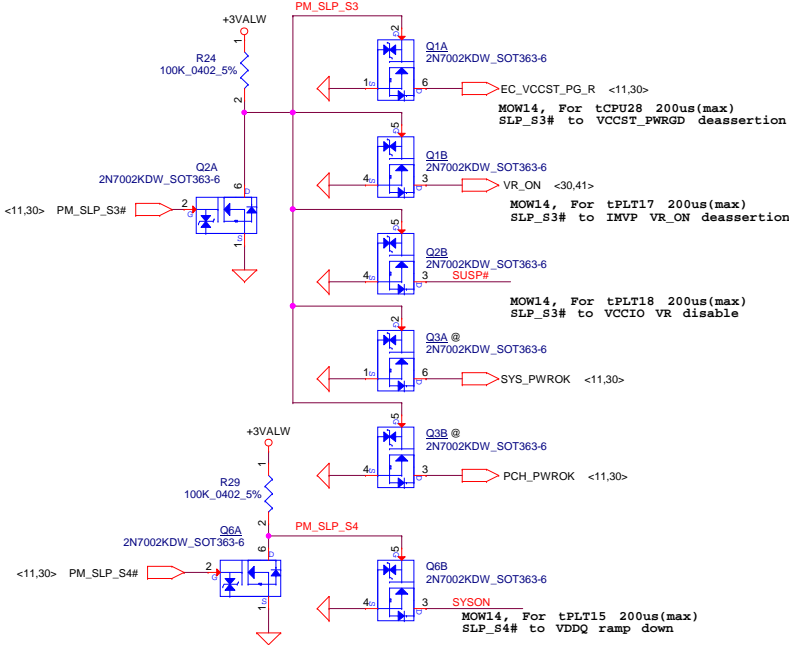


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				Date: Monday, June 12, 2017	Rev 1A Sheet 32 of 46

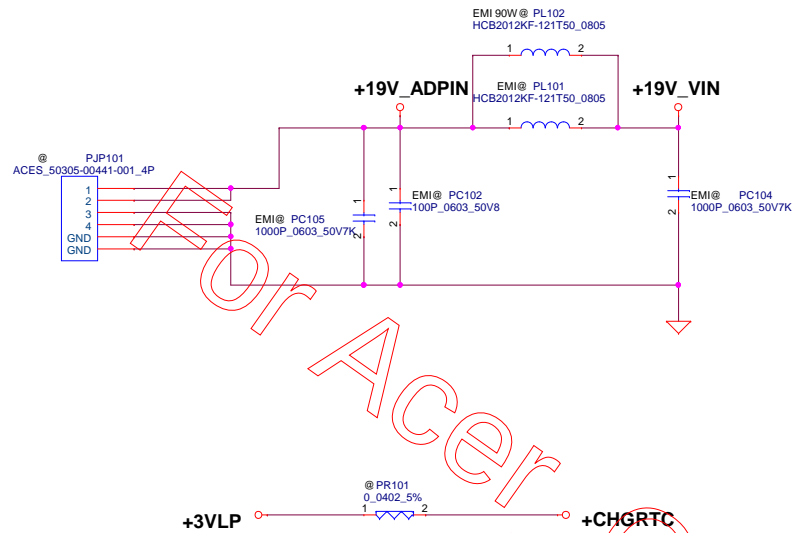
DC Interface



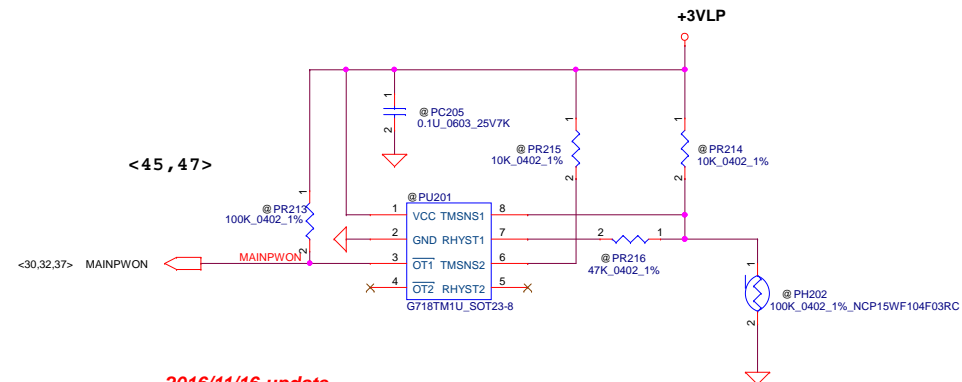
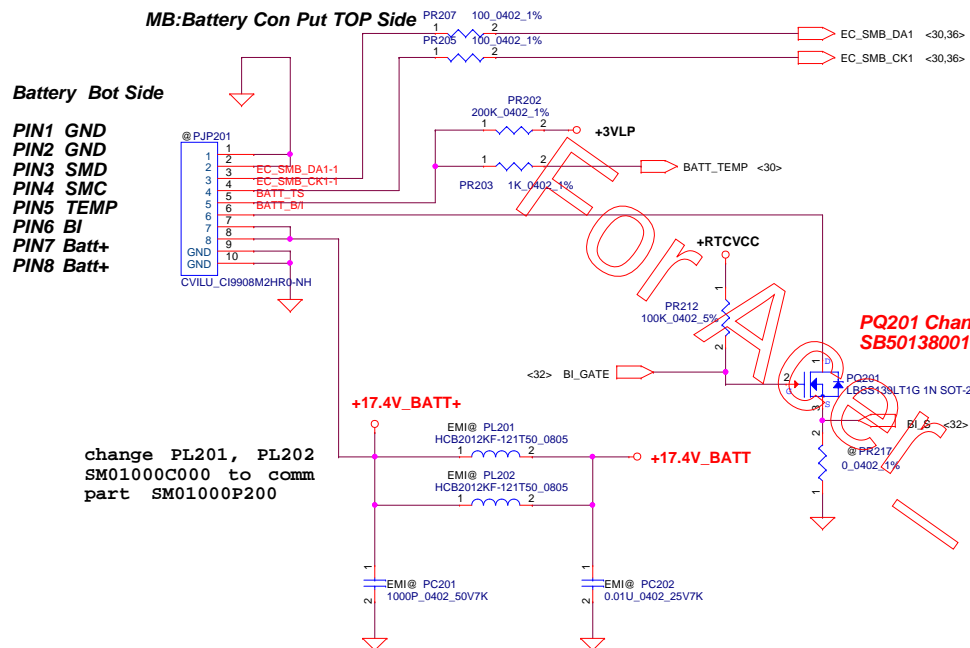
For Power ON/Off Sequence



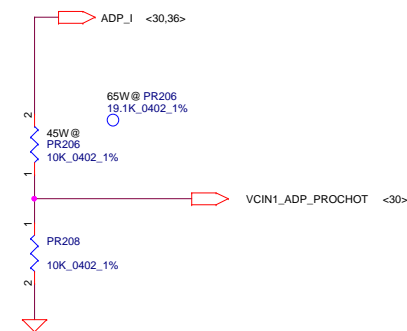
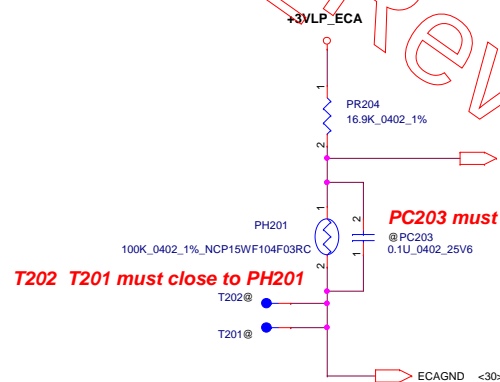
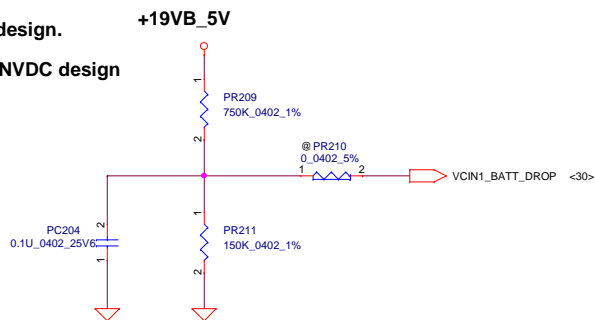
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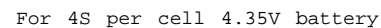
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				Size	Document Number
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VAL50/ZAL20 Battery is 3-cell NVDC design.
B+=9V
Change PR12=50k if Battery is 2-cell NVDC design
B+=6V



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$$\begin{aligned} \text{VILIM} &= 20 \cdot \text{ILIM} \cdot \text{Rsr} \\ \text{ILIM} &= 3.3 \cdot 100 / (100 + 316) / 20 / 0.01 \\ &= 3.966 \text{ A} \end{aligned}$$

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Module model information

RT6575D_DMOS_single_V1.mdd
RT6575D_DMOS_dual_V1.mdd

H/S Rds(on):typ:12.4mOhm, max:15.8mOhm
Idsm(TA=25)=13A, Idsm(TA=70)=7.8A
Ploss=0.42W

L/S Rds(on):typ:9.1mOhm, max:11.6mOhm
Idsm(TA=25)=15A, Idsm(TA=70)=9A
Ploss=0.14W

CHOKE:4.7uH, DCR 35mOhm
Ploss=1.77W

Output capacitor ESR need follow
below equation to make sure feed back
loop stability
 $ESR=20mV \cdot L \cdot f_{sw} / 2V$

POK need pull high, it
will pull high on VS
transfer circuit

5V-OCP=13.5A
3V-OCP=8.9A

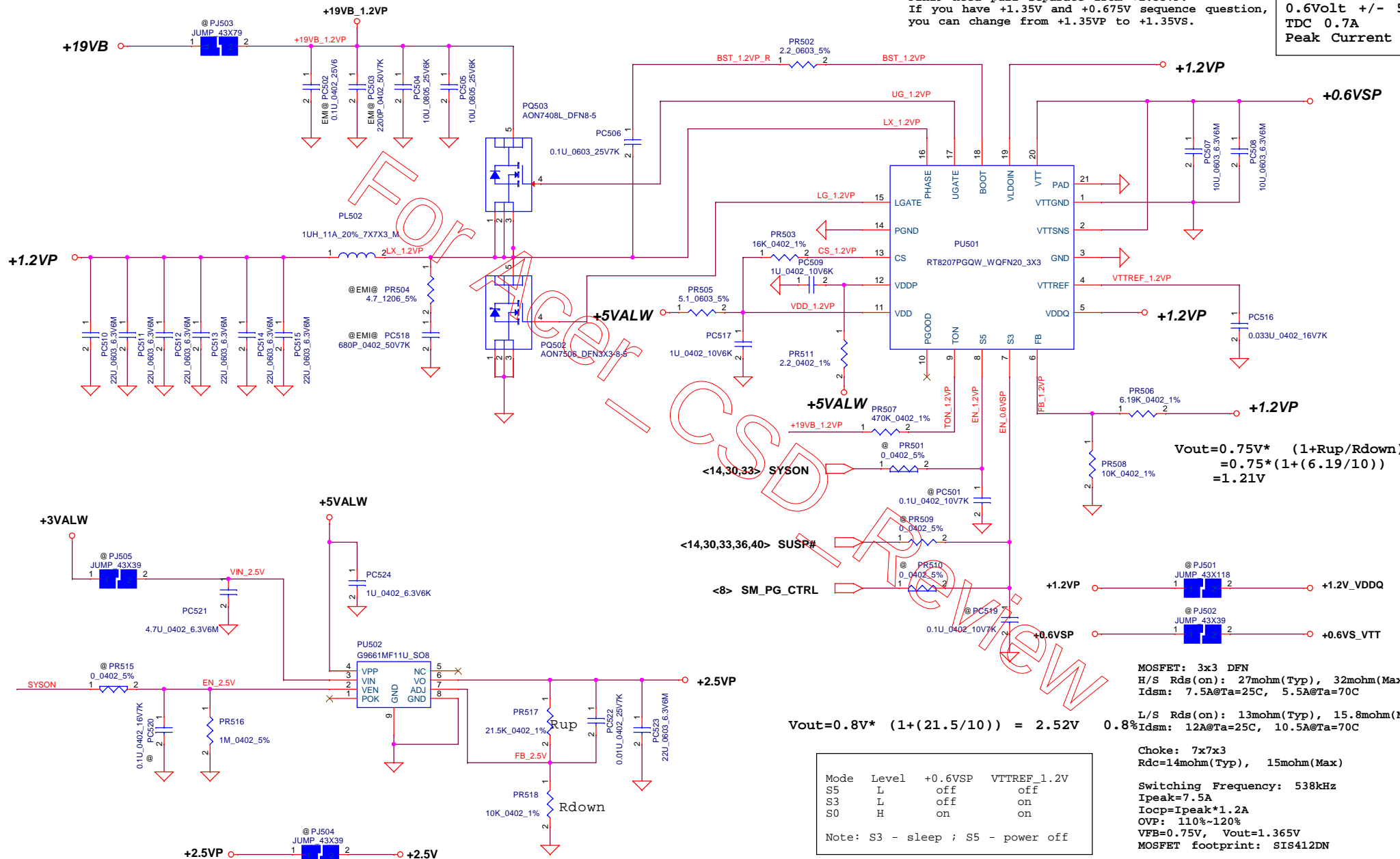
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schematic from A4WAS
IC change RT8207K

Pin19 need pull separate from +1.35VP.
If you have +1.35V and +0.675V sequence question,
you can change from +1.35VP to +1.35VS.

0.6Volt +/- 5%
TDC 0.7A
Peak Current 1A



MOSFET: 3x3 DFN
H/S Rds(on): 27mohm(Typ), 32mohm(Max)
Idsm: 7.5A@Ta=25C, 5.5A@Ta=70C

L/S Rds(on): 13mohm(Typ), 15.8mohm(Max)
0.8%Idsm: 12A@Ta=25C, 10.5A@Ta=70C

Choke: 7x7x3
Rdc=14mohm(Typ), 15mohm(Max)

Switching Frequency: 538kHz
Ipeak=7.5A
Iocp=Ipeak*1.2A
OVP: 110%-120%
VFB=0.75V, Vout=1.365V
MOSFET footprint: SIS412DN

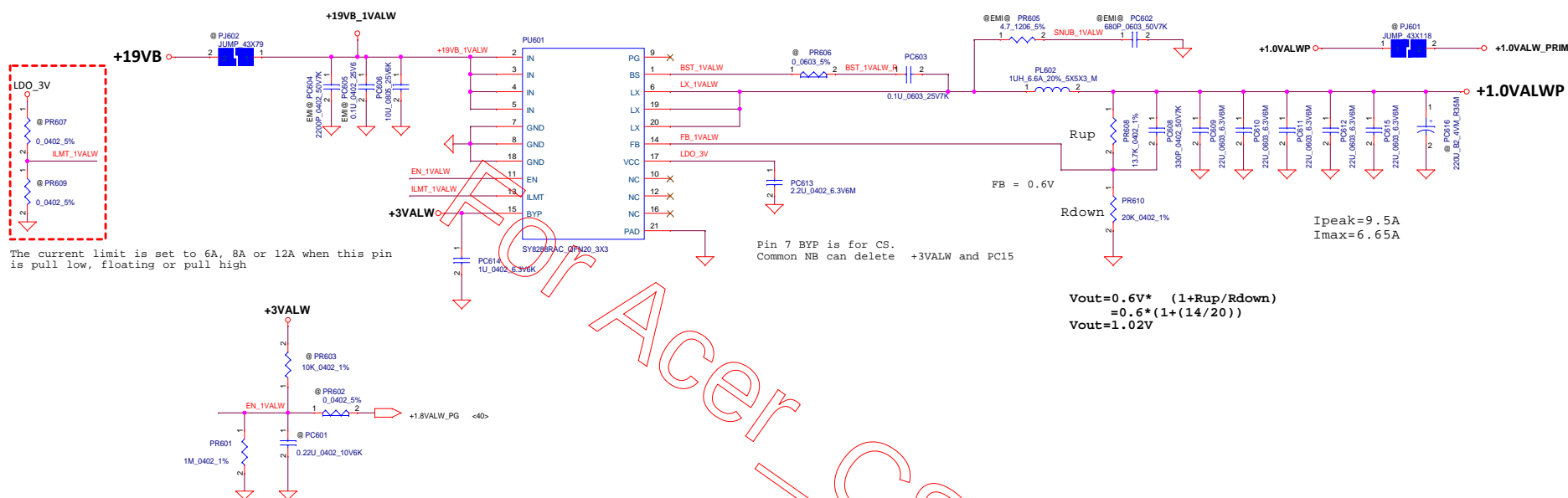
$$V_{out} = 0.8V * (1 + (21.5/10)) = 2.52V$$

Mode	Level	+0.6VSP	VTTREF_1.2V
S5	L	off	off
S3	L	off	on
S0	H	on	on

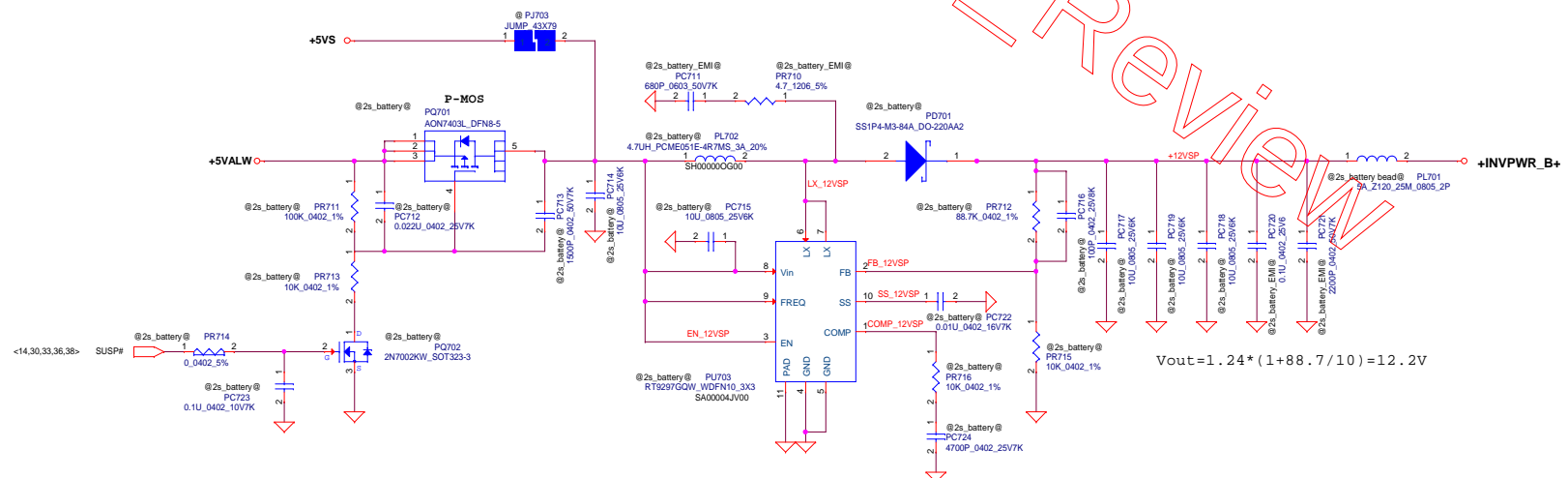
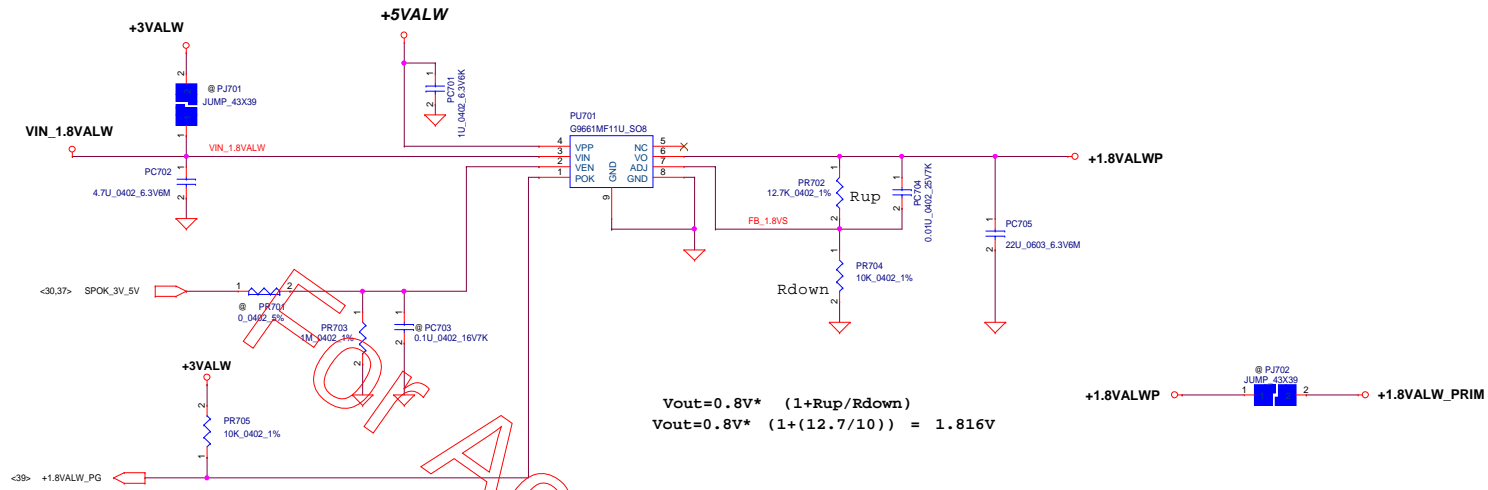
Note: S3 - sleep ; S5 - power off

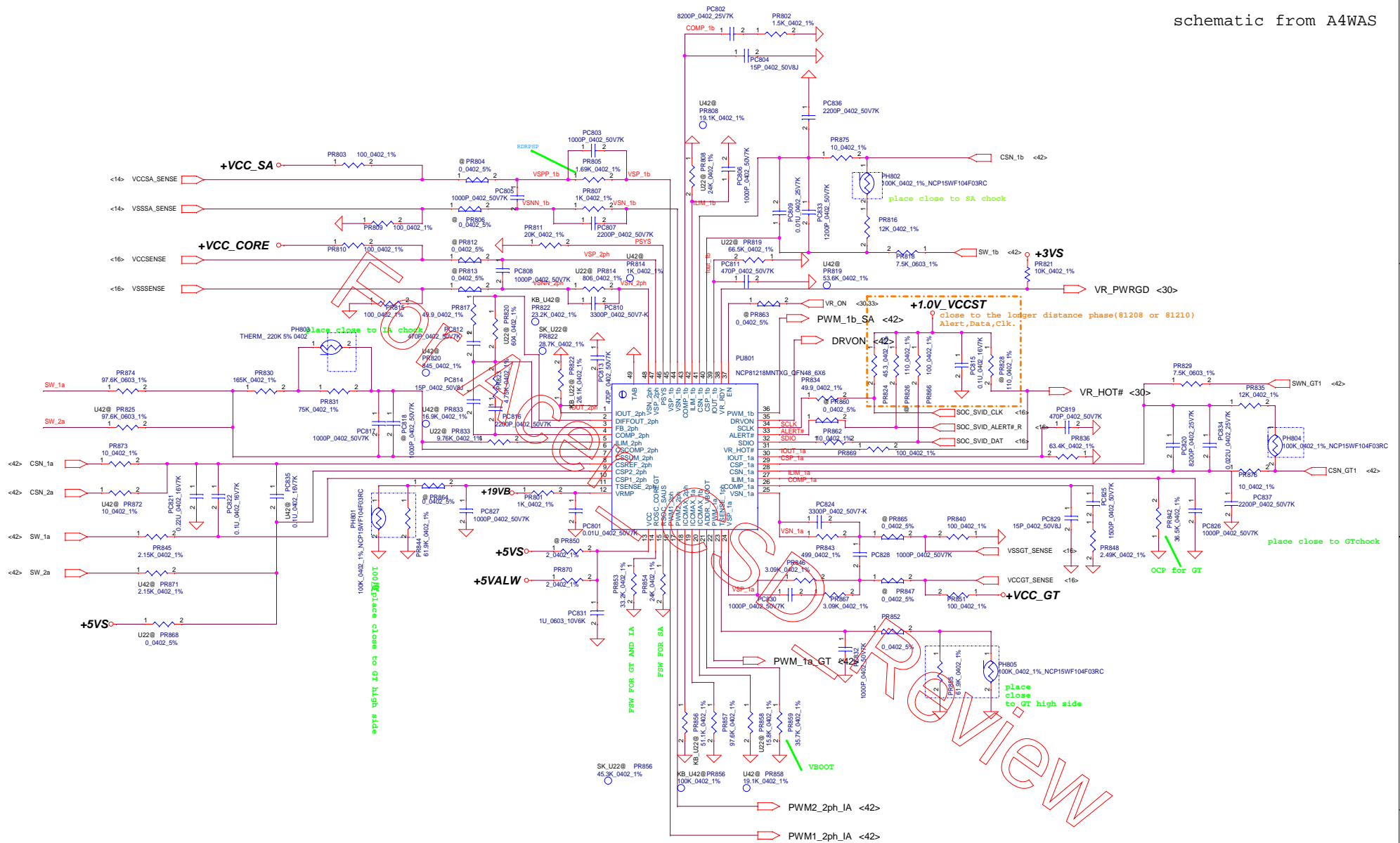
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EN pin don't floating
If have pull down resistor at HW side, pls delete PR702

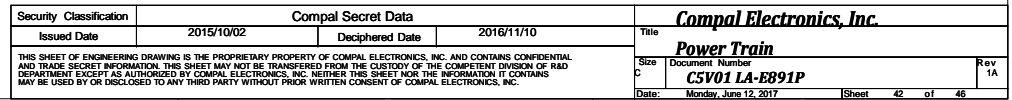


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Power Train





SA
pop:
22uF_0603*9
1uF_0201*7
unpop:
22uF_0603*3

220uF*1
22uF*36
1uF*9
0.47uF*4
unpop: 22uF*8
1uF*1

2016/10/26
VCORE Output Capacitor:
U42
22uF_0603*39
1uF_0201*35
220uF*3
UNPOP
22_0603*3

2016/10/26
VCORE Output Capacitor:
U22
22uF_0603*33
1uF_0201*35
UNPOP
22_0603*9
220uF*3

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		Date		Date	
		10/26/2016		10/26/2016	

Version change list (P.I.R. List)

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for PWR

Item	Fixed Issue	Reason for change	Rev.	PG#	Modify List	Date	Phase
01	prevent part damage				PC410 and PC411 change to 0603 size	1/3	DVT
02	reduce part count				PR515, PR804, PR806, PR812, PR813, PR865, PR847, PR860, PR876, PR863, PR875, PR901, PR912, PR904, PR913, PR914 change to R-short	1/3	DVT
03	voltage level too high	3.37V change to 3.33V			PR402 change to 13.3K from 13.7K	1/3	DVT
04	voltage level too high	1.02V change to 1.011V			PR608 change to 13.7K from 14K	1/3	DVT
05	SMT	close SMT stencil problem			PJ9001, PJ9002, PJ9003 change to 0.2m ohm	1/3	DVT
06	CPU transient	meet CPU spec			PR805 change to 1.69K from 1.78K PR814 change to 806ohm from 1K PR874 change to 97.6K from 93.1K PC821 change to 0.22u from 0.1uF PC820 change to 8200P from 0.01uF PR836 change to 63.4K from 69.8K PR846 and PR867 change to 3.09K from 3.32K PC9002, PC9003, PC9099, PC9098, PC9014, PC9091, PC9048 change to dummy	1/14	DVT
07	DC S5 power consumption	meet DC S5 2.5mA spec			PR209 change to 750K from 10K PR211 change to 150K from 2K	1/14	DVT
08	prevent shortage				PL907 change to common part SH00001ED00 PQ502 change to AON7506	1/14	DVT
09	meet panel spec voltage	remove boost circuit			PQ701, PQ702, PR711, PR712, PR713, PR715, PR716, PC712, PC713, PC714, PC715, PC722, PC724, PL702, PD701, PU703, PC717, PC718, PC719, PC721, PL701 change to un-pop	1/14	DVT
10	reduce part count				PR852 and PR864 change to R-short	1/14	DVT
11	spok voltage level				PR407 change to 20K ohm from 100K	1/24	DVT
12	Change to 5V OCP setting				PR406 change to 105K ohm from 107K	3/1	PVT
13	for CPU transient				PU901 and PU902 change to NCP81151MNTB6_DFN8_2X2 PU903 change to NCP81253MNTB6_DFN8_2X2 PR908 change to R-short from 10 ohm PR876, PR875 change to 10ohm from R-short PC837, PC836 change to pop to 2200P	3/1	PVT
14	from soucer suggest for USB 5V Level				PC901 change part number SF000007700 from SF000007200 PR401 change to 31.6K from 30.9K	3/4	
15	for U42 modify				PR808 change to 19.1K PR814 change to 1K PR820 change to 845 ohm PR857 fix to 97.6k PR858 Change to 19.1K PR836 fix to 63.4K PR819 Change to 53.6K PR320 Change to 499ohm PC323 Change to 2.2uF PC9100 change to unpop		

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HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
1	25	12/22	1.0	Reserved CA32 for DMIC_CLK (EMI request)	reserve CA32 10P_0402_50VBJ
2	23	12/22	1.0	Net error	change RC150,RC151, RC153, RC224 PU to +3VALW_1.8VALW_PGPPD
3	12	12/22	1.0	+1.8vs power sequence f i net une	CC104 Change to 0.1uF ,RC168 Change to 49.9K ohm
4	11	12/30	1.0	Crystel 25MHz Cap. value follow vendor suggest	CC12,CC13 Change to 27pF (SE071270J80)
5	11	12/30	1.0	Crystel 32.768kHz Cap. value follow vendor suggest	CC16 Change to 6.8pF (SE07168AC80)
6	14	12/30	1.0	Change load swith part number	UC6 change to SA000070V00(AOZ1334DI-02_DFN8-7_3X3)
7	29	1/12	1.0	Type-C change connector	JUSB4 Symbol change to LOTES_AUSB0249-P001A_24P-T
8	8	1/12	1.0	X1 Code BOM Change	UC7 Change to SA00007WE00
9	31	1/12	1.0	Modify BOM structure	LK2 Change to @EMI@ , DK2 change to @ESD@
10	32	1/12	1.0	ME Drawing modify (DFB issue)	H30,H29 Change to H_3P2
11	23	1/12	1.0	For SD Card write protect issue	add QL1 & RL21 for SD_WP inverter circuit , reserve RL20 , RL22 (unpop)
12		1/13	1.0	Part count reduce	RM9,RO3,RS10,RM23,RS37,RS38,R1,R2,R3,R35,R36,R37, R38,R39,R40,R41,R34 change to R-short
13	31	1/13	1.0	Modify BOM structure	LK2 Change to @EMI@ , DK2 change to @ESD@
14	28	1/13	1.0	X1 Code BOM Change	DS21, DS1 ,DS2 ,DS3 ,DS4 Change to SC300002800 (USB3.0)
15	19	1/16	1.0	Customer request for ESD protect	RD202 Change to 0 ohm (DDR_DRAMRST#)
16	11	1/16	1.0	Customer request for ESD protect	reserve CC131 on EC_VCCST_PG
17	11	1/16	1.0	Customer request for ESD protect	add RC20 10_0402_5% ohm (PCH_PWROK)
18	15	1/16	1.0	Customer request for ESD protect	POP CC123 AND Change to 10U_0603
19	11	1/16	1.0	Cap. package Change	CS24 Change to 0402 package
20	26	1/17	1.0	remove HDD FFC co-lay	remove JHDD1 symbol
21	26	1/19	1.0	EMI part count reduce	RS1,RS2,RS3,RS4,RS5,RS6,RS7,RS8 Change to R-short
22		1/19	1.0	DFx review co-lay unused pin need to cover solder msk	JC1,LS1,LS3,LS4,LS6 cover solder mask (footprint update)
23	28	1/19	1.0	Bom Change , pull up resistor change to 100K ohm	RS20 Change to 100K ohm , RS40,RS41 Change to 100k ohm(unpop)
24	29,22	1/23	1.0	Change BOM part number	POP DY2,DY3 , Bom change to SC300002800
25	14	1/23	1.0	ESD request change BOM	POP CM15 & Change to 1000p Cap.
26	14	1/23	1.0	Follow Intel design guide	Add CC58 10U_0603
27	26	2/3	1.0	Parade SATA Re-driver EQ setting TX RX 7.4dB	POP RO17,RO18,RO19,RO21
28	22	2/6	1.0	BOM Change (ESD)	DY1 Change to SC300001G00
29	26	2/7	1.0	Fine tune TI SATA Re-driver EQ set t i g	POP RO17,RO18 (4.7K ohm) POP RO19,RO21 0ohm (TI re-driver GND Pin)
30		2/8	1.0	Acer ESD protect request	POP CC65,CC130,CC53,CC131,CS24(0.1uF) , CC50 (1000pF)
31	25	2/8	1.0	EMI request DMIC_CLK 0ohm change to Bead	RA34 change to SM01000NY00
32	29	2/16	1A	Change Cap. material for Z-High issue	CS25 Change to SGA00009M00 (H=2.1mm)
33	25	2/20	1A	Update BOM Structure	Change RA34 ,RA35 BOM Structure to EMI@
34		2/20	1A	For acer ESD protect request	Add CC132 & CC50 , CC53, CC131,CC65,CS24,CC132 Change to 1000P
35	11	2/20	1A	BOM Change	CC130 change to unpop
36	18	2/20	1A	Co-lay for Intel U42	Add RC237 R-short , RC182,RC183 R-short change to 0ohm(Reserved)
37	13	2/20	1A	Cancel USB20_Port9	remove LS24 , USB20_P9/USB20_N9 Add test point
38	26	3/1	1A	Update Type-c footprint	JUSB4 change symbol to LOTES_AUSB0181-P001A
39	12	3/2	1A	For BIOS Identify U22 , U42 CPU	RC215 Change BOM Structure to U22 / RC214 Change BOM Structure to U42
40	8	3/2	1A	Update DAZ / PCB Part number	DAZ Change to DAZ20X00101 , PCB Change to DA8001AT01A
41	9	3/2	1A	BIOS ROM Change Main source	UC2 Change to SA000039A40

HW Schematic chang list (P.I.R)

Item	Page	Date	Rev.	Reason for change	Modify Item
42	11	3/28	1A	Crystal damping resistor adjust	RC235 , RC236 change to 33ohm 1%
43	18	3/28	1A	Crystal damping resistor adjust (U42)	RC233 , RC234 change to 33ohm 1% , CC128 ,CC129 Change to 27pF
44	8	3/28	1A	RCOMP [0] 121 ohm for Mixed MD and SO-DIMM	RC38 Change to 121 ohm
45	8	3/28	1A	Update DAZ PN & Add U42 PN	DAZ change to DAZ20X00102 ,Add U42 QN5D@ / Q15C@
46	8	3/28	1A	Change ESD Main source	DYI Change to SC300002900
47	8	4/17	1A	Add D7W01 Project ID setting	RC207 / RC213 BOM structure D7W01@
48	30	4/17	1A	Add D7W01 Board ID setting	RB4 27K ohm for EA17PVT@ , RB4 33K ohm for EA17MP@

For Acer - CSD - Review